R6500

MICROCOMPUTER SYSTEM

HARDWARE MANUAL

R6500

Rockwell International

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PREFACE

The Rockwell R6500 Microcomputer System combines the best features of second-generation microcomputers into a product line that is a leader in both price and performance. A growing array of products and a unique microprocessor (CPU) family provide the R6500 System user with answers to the most complex microcomputer design problems confronting today's programmers and designers.

Integrated circuit fabrication techniques have moved microcomputers to the forefront of complex, sophisticated components. The R6500 System benefits from an advanced but proven integrated circuit process technology which is directly responsible for the high-performance characteristics obtainable in the single-supply, 5-volt usage of the R6500 System.

The N-channel, silicon gate circuit technology which is applied throughout the R6500 System is further enhanced by use of "depletion loads," to provide greater speed, lower power, and smaller chip size than previous processing approaches. Ion implantation techniques are basic elements in providing control and stability of all processing parameters necessary to achieve the electrical characteristics of the R6500 product line. These characteristics provide a price/performance combination which establishes the R6500 family as the product offering best meeting the economic and technical demands of today's system designs.

A word of explanation is in order regarding the R6500 Microcomputer System's microprocessor (CPU) "family" concept, since it is around this family that the R6500 System is built.

The R6500 System's microprocessor (CPU) family includes a series of 8-bit devices which offer the customer a wide range of options and capabilities. For the single-application customer, a varied selection of devices is at his disposal in choosing the one which best meets his specific needs. The "microprocessor family" concept has an even greater impact on the user who has a variety of applications, each of which can best be served by a specific

member of the family. It is important to this user that all of the different microprocessors he selects maintain compatibility – both hardware (from the standpoint of bus and electrical specifications) and software. The R6500 System product line offers the first microprocessor (CPU) family to achieve such a level of compatibility because it was indeed conceptualized as a totally software and hardware compatible family of microprocessors (CPUs) offering a range of performance options from which the designer can select. The R6502 and R6512 are the two 40-pin members of the family, each offering 65K bytes of addressable memory. The R6503 through R6507 and R6513 through R6515 are 28-pin versions with various options of addressing capability and control functions from which to choose.

The R652X Series represents Peripheral Input/Output devices, the first being R6520 which is a direct replacement for the Motorola MC6820 Peripheral Interface Adapter (PIA). The second device of this series is the 6522 Versatile Interface Adapter (VIA). Subsequent members of this series will include devices with expanded I/O capabilities.

The R653X Series represents combinational devices – those consisting of various tradeoffs in RAM, ROM, I/O, and Timing. The first of these is the R6530 which contains 1K bytes of ROM, 64 bytes of RAM, an Interval Timer and 16 I/O lines. The second is the R6532 RAM/IO/Timer with 128 bytes of RAM, an Interval Timer and 16 I/O lines. Subsequent products in this series will provide the customer with different combinations and new implementations of I/O, Timing and Memory.

All of the R6500 product-line subsystems utilize the same fabrication techniques and meet identical electrical specifications. With this family of compatible products at his disposal, today's designer has available the elements necessary to develop a system configured to meet the most demanding tasks.

The R6500 family is compatible with standard Random-Access Memories (RAMs), including the 2102, 2111, 2114 and the 2115.

To allow for minimum I/O cost and maximum user flexibility, all of the R6500 products are compatible with the M6800 bus structure.

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SECTION 1

THE R6500 MICROCOMPUTER SYSTEM

The past several years have seen the development of an exciting new concept in electrical design. The microcomputer started out as a relatively simple, difficult-to-use programmable device capable of handling simple control or computational problems. However, it has since matured into a powerful, inexpensive, easy-to-use device capable of controlling all but the most complex of systems.

Conventional system design is rapidly being revolutionized by the component that forms the heart of the microcomputer -- the large-scale, single-chip programmable microprocessor (CPU). Three primary attributes of microprocessor-based systems are bringing about this revolution:

1. Microprocessors allow a significant reduction in overall systems cost for products currently in production. Re-design of products around the microprocessor is permitting many manufacturers to develop or maintain a price advantage over competitors.
2. The reduction in cost of microcomputer systems is opening up vast new markets for microprocessors. A great number of systems which were simply impossible or were at best impractical, are being designed and marketed today using the modern, low-cost microprocessors.
3. At the same time that the price of microprocessors is dropping, their capability is rapidly expanding, thus allowing them to be designed into more systems than ever before.

Anyone contemplating a new design or trying to reduce cost in an existing design must first ask himself if a microprocessor will solve his problem.

The success of the microprocessor is based on the fact that it permits the design engineer and programmer to apply their expertise in solving a multitude of design problems using cost integrated effective circuits. A small number of large integrated circuits can be configured to solve design problems from the simplest to the most complex.

If the same integrated circuits are employed to solve a multitude of unique designs, the first question one must ask is, "What makes the designs unique?" The answer is: Programming. Although many different designs may share common hardware, each has its own unique program. This brings us to another very important characteristic of microcomputers. The integrated circuit which makes each system unique is the "Read-Only Memory" (ROM) which stores the system program. It is relatively easy for the integrated circuit manufacturer to establish the particular pattern which uniquely defines the data in a ROM. As a result, the typical charge for "designing" a ROM is generally less than 10% of the cost of designing a totally custom logic chip. Further, the user benefits from a high-volume standard product which is still unique for his own application due to the "customization" of one element of his system.

It will probably surprise many designers, approaching the subject of microcomputer design for the first time, to discover that designing a system around a microprocessor is much the same as designing around conventional logic. The total approach is the same: the process differs only in the implementation of each step.

A brief examination of the system design process will help to put microcomputer design in perspective and will also assist in clarifying the purpose of this manual. One can expect to perform the following steps in designing a microcomputer system:

1. Define the requirements of the system. What functions should it perform?
2. Define basic system components.
3. Complete design details.
4. Build and test prototypes.
5. Finalize design and begin production.

Step 1 is true for any system and, in general, for any product. Step 2 is the first point of departure for microprocessor-based designs. It is at this point that the designer must consider the possibility of using a microprocessor in his system. For the very cost-sensitive application he must look very carefully at total systems cost. Can a microprocessor do the job within the price constraints imposed? At the other end of the design spectrum, the system designer must evaluate the capability of microprocessors to assure himself that the available devices can in fact perform the required function. Will a microprocessor be fast enough to run the system? Will the system require more than one processor?

The purpose of this manual is to teach the designer how to effectively configure a microprocessor-based system and to evaluate the performance of the system. After this step, the design will be completed by development of the system program. Implementation of the system program is discussed in the Program Manual.

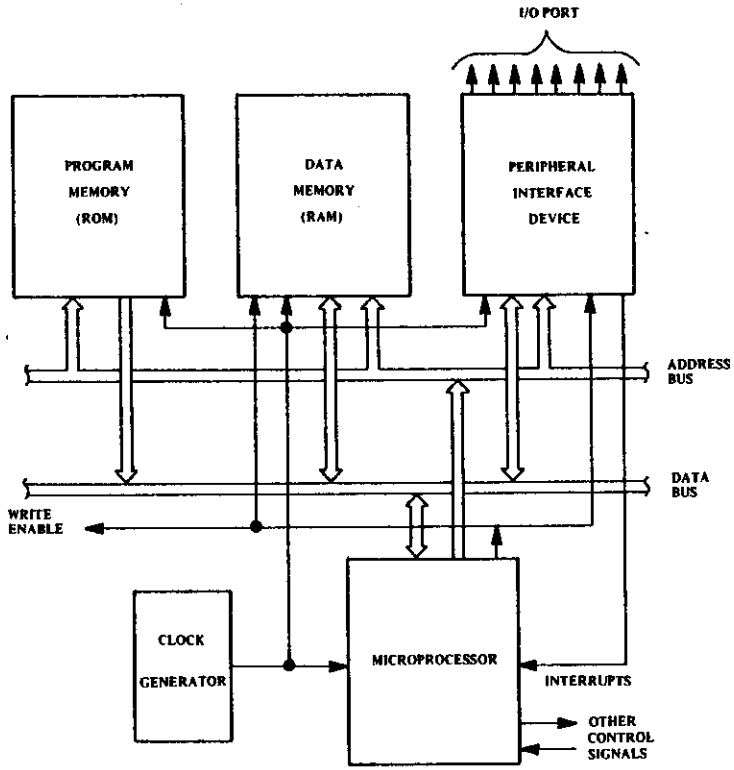
1.1 INTRODUCTION TO MICROCOMPUTER SYSTEMS

1.1.1 Organization of a Microcomputer System

Figure 1-1 illustrates the basic organization of a microcomputer system. It is important that the designer understand the operation of each component as well as the operation of each data path in the system. Each of these is discussed separately below. In addition, the following discussion describes the operation of the overall system and the use of the various signal paths.

1.1.2 Basic Operation

The microcomputer is a system which can be characterized as very simple in its detail and very complex in its overall operation. It carries out rather complex tasks by performing a large number of simple operations. Control of the system is primarily the responsibility of the processor. By putting out addresses to program memory, it controls the sequence of operations performed, and by interpreting and executing the instructions which it receives from the program memory it controls the actual operations carried out by the system. The processor is by far the most complex device in the system. For this reason, it is important to overall system cost that this part stay the



Organization of Microcomputer System

FIGURE 1-1

same for many different applications. In this way, the relatively high development cost can be shared by thousands of users. In addition, those thousands of users can all benefit from the economics of large-scale production.

The processor causes the system to perform the desired operations by reading the first instruction in the program, and performing the very simple task dictated by the specific pattern of bits in this instruction (referred to as "executing" that instruction). It then goes on to the next instruction in the program and executes it. This simple operation of fetching an instruction and executing it is performed over and over, each time on the next instruction in sequence. In this way the program instructs the processor to bring about the desired system operation.

1.1.3 Addressing Terms and Concepts

Before entering into a detailed discussion of the system operation, it would be useful to define a few terms and to introduce a few concepts concerning addressing. This should assist in an understanding of the detailed discussions which follow.

BIT

The term "Bit" is a general term referring to anything that can be assigned to binary value, i.e., anything that can be given a value of 0 or 1. Thus, an eight-bit data bus is a set of 8 lines which can be assigned a value of logic 0 or logic 1. On these lines, the logic values are represented by two different voltages or currents. Similarly, a 16-bit binary display can be built with 16 individual lamps. The logic 1 is represented by the lamp being on.

In this text, reference is made to an 8-bit data bus, a 16-bit address bus, 4 bits of data, 8-bit registers, etc. In all cases, definition of a bit remains the same.

ADDRESS SPACE

The concept of an address space is very useful in understanding microcomputer systems. The term "address space" refers to the total set of addresses which the microprocessor can generate. For example, if a processor had only 4 address lines, it could generate the addresses 0 - 15 (binary 0000

to binary 1111). This would not be adequate for any microcomputer operation and, consequently, the typical processor has between 12 and 16 address lines. Since each line can assume a value of 0 or 1, these devices can usually address from 4,096 to 65,536 separate addresses. Figure 1-2 contains a pictorial representation of the address space available in a typical 8-bit microcomputer with 16 address lines. In addition to the general address space, this figure introduce the PAGE concept discussed below.

THE ADDRESS PAGE

The concept of a PAGE in memory is very important in 8-bit microcomputer systems. The internal organization of an 8-bit processor is around 8-bit registers, 8-bit parallel data paths, etc. Most arithmetic operations, logic operations, etc. take place on 8 bits of data at a time. Similarly, the 16-bit counter which determines which instruction is being executed is actually divided into two 8-bit busses. One contains bits 0 - 7 (low-order address bits), and the other contains bits 8 to 15 (high-order address bits). With this in mind, one can think of the address space shown in Figure 1-2 as consisting of 256 blocks, each consisting of 256 specific address locations. Each of these blocks is referred to as a "PAGE" of memory. The high-order 8-bits of the address (ADH) therefore indicate in which page the address is located, and the low-order 8 bits (ADL) indicate a specific address on that page.

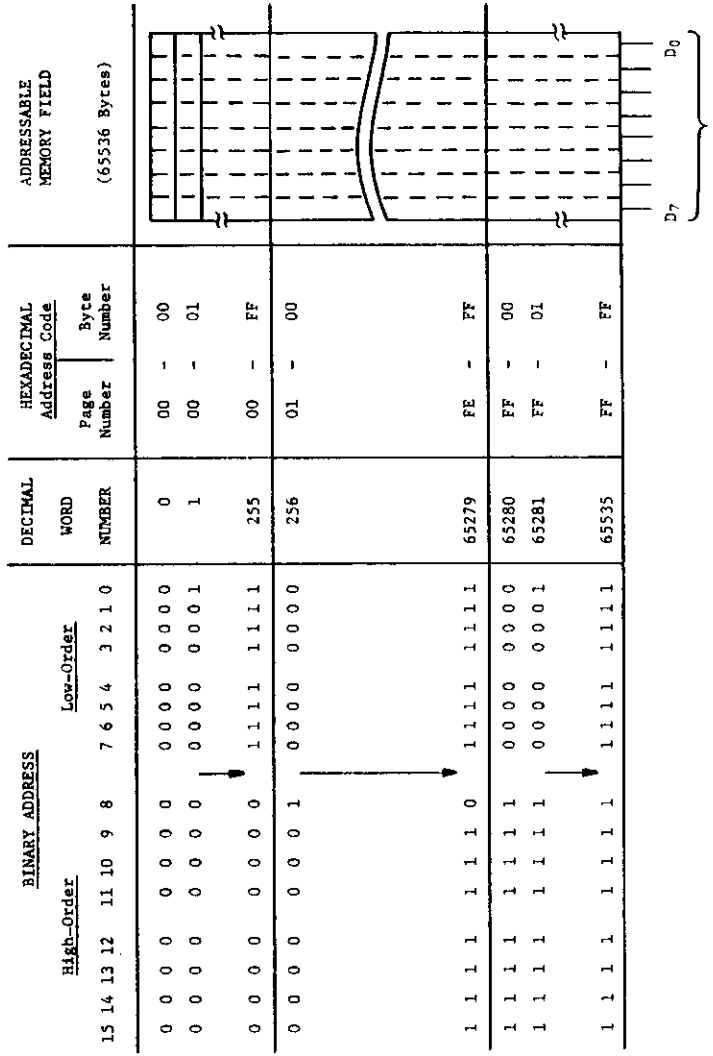
The first page in memory (ADH = 00) is referred to as page 0. The next-high-order page (ADH = 01) is referred to as page 1, etc.

1.1.4 System Components

The block diagram in Figure 1-1 shows the basic components which comprise all microcomputer systems. Each block in the diagram may consist of one or more integrated circuits and, in fact, several functions may be combined into single chips. However, the basic operation of each remains the same.

CLOCK GENERATOR

The clock generator produces a continuous waveform which is normally used to control all signal transitions within the system. It acts as the "heart" of the system. In the typical microcomputer system the address bus will change during one half of the clock cycle, and the data will be



Address Bus and Relation to Memory Field
FIGURE 1-2

transferred during the second half. In addition to interpreting the address, data and control lines, the processor and support chips must also examine the system clock to know when to put out data or when to latch in data generated by another device.

PROGRAM MEMORY

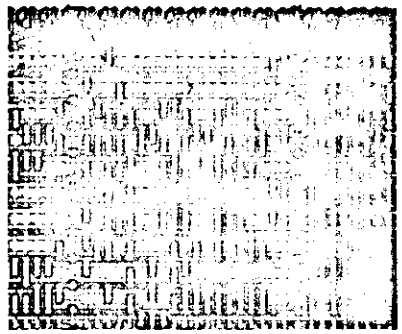
The program memory stores the sequence of instructions which comprise the system program. Like any memory, this unit puts a pattern of 1's and 0's on the data bus in response to the address on the address bus input. Each unique address selects a set of 8 binary bits and places these data on the data bus. Note that it does not matter where the address is generated or where the data are used; the memory simply obeys the rule that, given an address, it will put the corresponding 8 bits of data on the data bus.

A unique characteristic of most microprocessor-based systems is that the program is usually stored in Read-Only Memories (ROMs). The data are stored in a fixed pattern of bits in the memory. Figure 1-3 shows a section of a semiconductor ROM.

Since the data are stored in the physical configuration of the device, the data will not be lost when power is disconnected from the chip. In addition, it is necessary only to insert the device into its socket to provide the system program. The term "Read-Only Memory" refers to the fact that, in system operation, it is impossible for the processor to cause data to be stored in the device. The processor can "READ" the data stored in the device during the manufacturing process. "READING" a memory involves the simple process of supplying an address to the device to obtain the corresponding 8 bits of data on the data bus.

DATA MEMORY

For temporary storage of input data, the results of arithmetic operations, etc., the microcomputer uses a Read/Write Memory, commonly referred to as a RAM (Random-Access Memory). The processor can store data in the RAM (called "WRITING" the RAM), or it can read back the data it has stored. As in the ROM, each address corresponds to eight memory cells.



Portion of Read Only Memory Matrix
FIGURE 1-3

However, in a RAM the data must be placed into the memory by the processor and are stored in cross-coupled latches. Turning off the power to a RAM will cause the loss of all data stored there, and the data are said to be "volatile." Data in a ROM are not lost when power is disconnected from the device and the stored data are referred to as "non-volatile".

"WRITING" data into a RAM takes place when the Write-Enable signal goes to the write state. At this time the data on the data bus will be stored into the eight memory cells corresponding to the address on the address bus. The processor can READ this same data by supplying the proper address and keeping the Write-Enable line in the Read state.

INPUT/OUTPUT DEVICES

The Input/Output Devices are the circuits which interface the printer, keyboard, displays, etc. to the processor. These allow the processor to read data from the keyboard, to test the state of sensors and switches, and to display or to print the results of internal operations.

No matter where data are generated, they must be, in the form of 1's and 0's before the processor can work with them. Similarly, actions to be initiated by the processor must be triggered by 1's and 0's transferred by the processor to a set of output lines.

The transfer of data from the processor to an output device is usually accomplished by "WRITING" the data out in much the same manner as the processor writes data into RAM. Each set of 8 input or output lines (referred to as "PORT") is given an address, and the processor simply writes data to that address. For each "1" written out to the peripheral port an output is set high, and for each "0" the corresponding output is set low.

Although the basic concept of peripheral control is simple, the actual implementation of these interfaces can involve many sophisticated techniques designed to allow the processor to maximize its ability to control peripherals and perform internal operations concurrently. These techniques are discussed in detail in Section 3.

THE MICROPROCESSOR

At first glance it may seem strange to discuss the support chips in the microprocessor-based system before mentioning the processor. However, this approach is necessitated by the fact that most of the inputs and outputs on the processor are aimed at properly controlling the support chips and peripheral devices discussed above.

The address bus, the bidirectional data bus and the Write-Enable line allow the processor to exercise direct control over the rest of the system. The address bus puts out addresses to control the source or destination of data transfers. These addresses are derived from various sources within the processor. During the fetch of instructions from program memory, the addresses are usually derived from a counter which controls execution of sequential instructions. Addresses for data transfers between the processor and RAM are usually derived directly from the program or are calculated from the data in the program and data in internal registers.

The bidirectional data bus serves as a path for transferring data into and out of the processors. The direction of the data transfer is determined by the Write-Enable line.

Another special function found in modern microcomputer systems is the interrupt. This function allows the peripheral devices to directly affect the operation of the processor. When the interrupt signal is generated, the processor usually completes its current instruction and then, under program control, will respond to the interrupt. The importance of this function is that it allows the processor to execute the system program without requiring the system program to monitor the status of the peripheral device. The software which handles the operation of each peripheral will be executed only when required.

1.2 *INTRODUCTION TO THE R6500 MICROCOMPUTER SYSTEM*

The Rockwell R6500 microcomputer system consists of the 40-pin R6512, microprocessor; the 40-pin R6502 microprocessor, which has clock drivers on-chip; and eight 28-pin processors, the R6503 through R6507 and R6513 through R6515. Each of these devices is aimed at a specific range of applications. Therefore, it is important to develop an understanding of the capabilities of each and the differences between them.

The R6512 has application in existing M6800 systems where conversion to the R6500 system is to be performed. This processor requires the full high-level two-phase clocks of the M6800 system. The R6502 is expected to find application in all new designs which require a full 16-bit address bus. However, in the small cost-sensitive system, the 28-pin processors can represent a savings both in processor cost and in printed circuit board area.

1.2.1 The Microprocessors

The R6502 should be used in all new designs which require the capability of the 40-pin processors. The clock drivers can be driven with a single TTL level square wave or with the internal oscillator. The frequency of operation of the internal oscillator can be set by attaching an R-C combination to the chip and, if the clock stability is required, by attaching a crystal between the oscillator and ground. This feature totally eliminates the problems encountered in generating MC6800-type clock signals.

The R6502 provides a full 16-bit address bus, 8-bit bidirectional data bus, and two interrupts. In addition, the R6502 provides a sync signal which indicates those cycles in which the processor is fetching an operation code from program memory.

Eight 28-pin versions of the processor are available. They differ in the number of address lines and the clock generation methods required, the number of interrupts provided. Having all three options available allows the designer to tailor his processor to his particular application.

The R6504 and R6507 provide a total of 13 address pins and can, therefore, address a full 8K bytes in its memory space. The R6504 provides only one interrupt request input, $\overline{IRQ}$; the R6507 provides a RDY input instead of $\overline{IRQ}$. The non-maskable interrupt ($\overline{NMI}$) is not included in the pinouts of this device.

The R6503 and R6505 provide one less address line. In the R6503 the missing address line is replaced with a second interrupt input, $\overline{NMI}$, and in the R6505 it is replaced by the RDY signal. All other functions on these processors are the same. The details of each of the pins are discussed in the following sections.

The operation of the various busses, control signals, etc. is identical on all R650X products, with all processors obeying the system specifications discussed in Section 1.2.2.

The R6513 is the slave (clocks driven in) version of the R6503, the R6514 is the slave version of the R6504, and the R6515 is the slave version of the R6505.

1.2.2 Bus Structure

The R6500 microcomputer system is organized around two primary busses. Each bus consists of a set of parallel paths which can be used to transfer binary information between the devices in a system. The first bus, known as the ADDRESS BUS, is used to transfer the address generated by the processor to the address inputs of the memory and peripheral interface devices. The processor is the only source of addresses in a normal system, so this bus is

referred to as "unidirectional." The address bus consists of 16 lines on the R6502 and R6512, allowing those processors to access (READ or WRITE) up to a total of 65,636 memory words, registers, etc. In the R6503 through R6507 and R6512 through R6515 the address bus contains fewer lines; therefore, they operate with a smaller "address space." This is discussed in detail in Section 1.1.3.

The data bus in the R6500 microcomputer system consists of an 8-bit bidirectional data path. These lines transfer data from the processor to the selected memory word, etc. during a WRITE operation and from memory into the processor during a READ operation. All data and all instructions are transmitted on the data bus.

The direction of the data transfers is controlled by the READ/WRITE (R/W) line on the processor. This line performs the Write Enable function described in Section 1.1.4. As long as the R/W line is high (> 2.4V DC), all data transfers will take place from memory to the processor (READ operation). This line will go low only when the processor is going to WRITE data out to memory.

As in most microcomputer systems, the timing of all data transfers is controlled by the system clock. The clock itself is actually two non-overlapping square waves. This two-phase clock system can best be thought of as two alternating positive-going pulses. This text will refer to the clocks as "Phase 1" and "Phase 2." A "Phase 1" clock pulse is the positive pulse during which the address lines change, and a "Phase 2" clock pulse is the positive pulse during which the data is transferred. The timing of the signals on the Address Bus, Data Bus, and R/W line is shown in Figures 1-4 through 1-7. All signal transitions are specified with respect to the Phase 1 and Phase 2 clock signals. In particular, the address lines and the R/W line will stabilize during Phase 1, and all data transfers will take place during Phase 2.

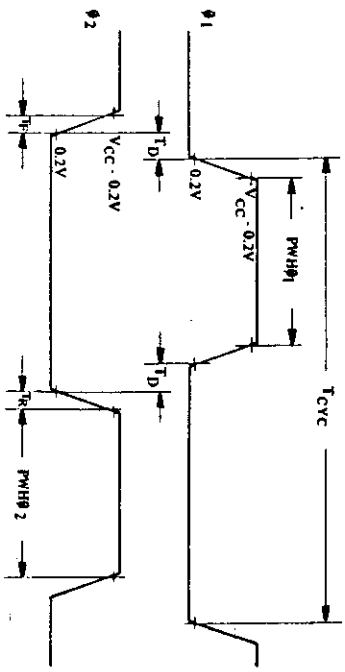
The specific timing specifications for operating at a 1-MHz clock rate are also given in Figure 1-4. Note that the sequence of operations will be the same for all processors. However, these timing specifications will change for devices which are specified to operate faster than 1.0 MHz.

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Cycle Time	T_{CYC}	1.0 us	--	--	µs
Clock Pulse Width Ø1 (Measured at V_{cc}-0.2v) Ø2	PWH Ø1 PWH Ø2	430 430	--	--	ns
Rise and Fall Times (Measured from 0.2V to V_{cc}-0.2V)	T_F, T_R	--	--	25	ns
Delay time between Clocks (Measured at 0.2V)	T_D	0	--	--	ns

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Read/Write Setup Time from R650X	T_{RWS}	--	100	300	ns
Address Setup Time from R650X	T_{ADS}	--	200	300	ns
Memory Read Access Time T_R T_{CYC} - (T_{ADS} - T_{DSU} - tr)	T_{ACC}	--	--	575	ns
Data Stability Time Period	T_{DSU}	100	--	--	ns
Data Hold Time	T_H	10	30	--	ns
Enable High Time for DBE Input	T_{EH}	430	--	--	ns
Data Setup Time from R650X	T_{MDS}		150	200	ns

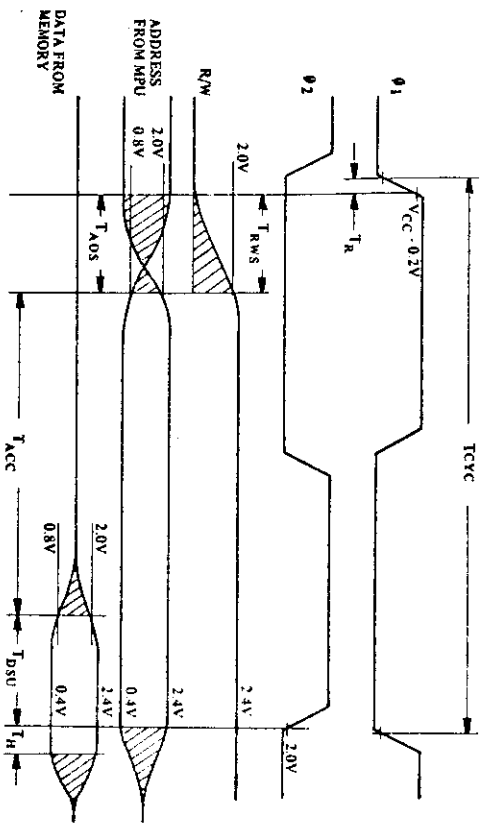
Clock and Read/Write Timing Table (1MHz Operation)

FIGURE 1-4



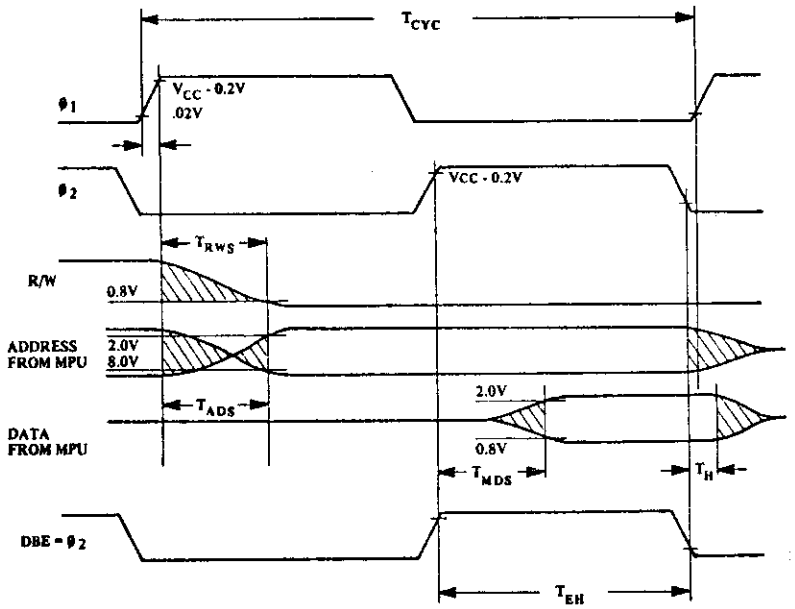
Two Phase Clock Timing

FIGURE 1-5



Timing for Reading Data from Memory or Peripherals

FIGURE 1-6



Timing for Writing Data to Memory or Peripherals

FIGURE 1-7

The address is guaranteed to be stable 300 ns after the leading edge of Phase 1, and the data must be stable 100 ns before the trailing edge of Phase 2. At 1.0-MHz operation, this allows the memory devices approximately 575 ns to make data available on the data bus. Although there are many factors which determine the actual data and address generated within the system, it is important to keep in mind that the basic operation shown in Figures 1-5, 1-6 and 1-7 does not change. These figures specify the system bus discipline which applies to all R6500 processors and support chips.

1.2.3 Interrupt Structure

Through the generation of processor interrupt signals, the peripheral devices (printers, keyboards, etc.) can request service from the processor. Although this technique is relatively simple in concept, the proper generation and control of interrupts is one of the most important problems which the designer will face. Total system capability can be greatly expanded if the processor is required to execute the peripheral software only when it is absolutely necessary. This is the goal of a well-planned interrupt structure. The interrupt structure is very much a systems sophistication problem since the entire system which must properly respond to the interrupt inputs. In fact, the actual signals to which the system must respond are usually applied to the inputs of a peripheral interface device. In this device, the interrupts are enabled, disabled and latched until the interrupt is processed. The peripheral interface device generates signals which meet the requirements of the processor interrupt inputs.

There are two interrupt input lines to the microprocessor, $\overline{IRQ}$ (Interrupt Request) and $\overline{NMI}$ (Non-Maskable Interrupt).

Since the requirements of the two interrupt inputs differ, they will be discussed separately below. The response of the processor to these inputs is very similar, however, after the interrupt is recognized. For this

reason, the internal operation of the processor during interrupt servicing is discussed in the detailed analysis of the processor chip. The present section of the manual concentrates on the system-level considerations which are required to assure proper operation of the interrupt structure.

APPLICATIONS FOR INTERRUPTS

One of the most important tasks facing the microcomputer system designer is the determination of those signals which will cause processor interrupts and those operations which will take place in response to the interrupts. A detailed discussion of these considerations is included in Section 3 of the manual; however, a few examples of interrupt-driven operations will be presented here to help the designer develop an understanding for why this technique is used extensively in microcomputer systems.

Example 1 -- A Fully-Decoded Keyboard

The problem of data entry is solved in many systems by a keyboard. In small systems, the interpretation of the binary code associated with each key can be determined by the processor. However, in large data terminals, the keyboard usually includes an encoder which generates the unique code corresponding to each key. When a key is closed, the corresponding code is placed on the output pins and a strobe signal is generated to indicate that a key has been pressed.

The keyboard represents a perfect candidate for interrupt-driven operation. The interrupts occur relatively infrequently and the operation to be performed is relatively simple. The keyboard strobe line is connected directly to an interrupt input on a peripheral interface device. Each time a strobe signal is generated, an interrupt occurs, the processor reads the data on the peripheral port into memory, analyzes these data, and then returns to the program that was in process. If no keys are pressed, the processor spends no time at all in servicing the keyboard.

Without the interrupts, the processor would have to read the keyboard data into memory periodically in order to detect an active key. This operation would be performed about every 50 to 100 ms. In addition to detecting an active key, the processor must make sure that each separate activation of a key is detected once and only once. (This is discussed later in this section.) This software is much more complex than the

simple interrupt routine. Another drawback of non-interrupt processing is that the processor is required to spend a periodic portion of its time on the keyboard. In many systems, this is not a problem, but in large terminals, etc., the time spent checking for keyboard strobes could be better spent in other operations. The designer must, therefore, ask himself if the system under development is such that the processor can perform the keyboard strobe checking function while still completing its other tasks.

Example 2 -- A Scanned Display

Although time is a major factor in determining the necessity of interrupts, the interrupt technique can also be extremely useful when performing parallel operations. A prime example of this can be found in a system which contains a digital display and/or printer.

A digital display is usually "scanned" in such a way that each digit is driven for a short period of time in sequence. The entire display is scanned at a rate faster than the eye can detect. However, it should be noted here that the display requires scan-related attention from the processor at fixed intervals. It is very difficult for the processor to calculate repetitive time intervals while it is performing its normal system program routines. The processor would much prefer to run the system program without consideration for the display time intervals -- only executing the display software only when it is required.

A solution to the above problem is the generation of processor interrupts at fixed intervals, employing an external counter or clock. Each time an interrupt occurs, the data for the next digit in the display are placed on an output port. The processor then returns to the program it had been executing.

Both of the operations described above represent solutions to system problems. Events which happen very infrequently, and events which must be performed in parallel with other events or in parallel with the main system program, should be seriously considered as candidates for interrupts. Additional considerations are described in Section 3 of this manual; however, it is important to note here that the typical system may have several sources of interrupts, each with its own timing and each with its own set of operations which must be performed in response to the interrupts.

INTERRUPT PRIORITIZING

After a careful analysis of the total system and a determination of all the sources of interrupts, the designer must ask himself, "What happens if more than one interrupt source requires attention at one time?" A priority level must be established between the various interrupt sources. Which ones must be taken care of within a very short period? Which ones can be put off for a while? This prioritizing and the technique for selecting among several concurrent interrupts is very important to the system operation and should be established early in the system development process.

The R650X-based system can employ several hardware methods of determining the highest-priority active interrupt. These usually involve using a special "priority encoder" which allows the processor to go directly to the software which services the highest-priority interrupt. After this is complete, it will go to the next higher priority and execute that software. However, the R650X family provides a much less expensive method of interrupt prioritizing -- the "polled" interrupt. With this technique, each time an active interrupt source is detected, the processor executes a "polled" interrupt program that interrogates the highest priority interrupt, then the next highest, and so on until an active interrupt is located. The program services that interrupt and returns to the "polled" interrupt program and continues to interrogate the next highest priority interrupt until all have been interrogated, or clears the interrupt disable to allow nested interrupts. The "polled" interrupt program is always executed when an interrupt occurs, so that all interrupts that occur concurrently will be serviced in order of priority level.

Several hardware techniques for prioritizing interrupts are discussed in Section 3 of this manual. The next section, however, describes the system interconnect which allows use of the simple "polled" interrupt.

SYSTEM INTERCONNECT FOR INTERRUPTS

In the simple "polled" interrupt technique for prioritizing interrupts, the interrupt software actually determines the highest-priority active interrupt. The $\overline{IRQ}$ or $\overline{NMI}$ interrupt request signals simply cause the processor to jump to the polling software.

For this reason, it is possible to "OR" the various interrupt signals together to form the signal for the processor. Any active interrupt source will then cause the processor to do the interrupt polling and

servicing operation. Provision for generation of this OR function is provided in the R6500 family peripheral interface devices. Since these peripheral adapters perform many of the enabling and latching functions necessary for proper interrupt servicing, the peripheral adaptor interrupt output then provides the actual signal which interrupts the processor. These interrupt outputs can be "wire-OR'd" by connecting them all together and then connecting this single line to the processor. This input should then be pulled to +5V with a resistor. Any one of the interrupt outputs on the peripheral adaptors can then pull this interrupt low. This simple configuration is shown in Figure 1-8.

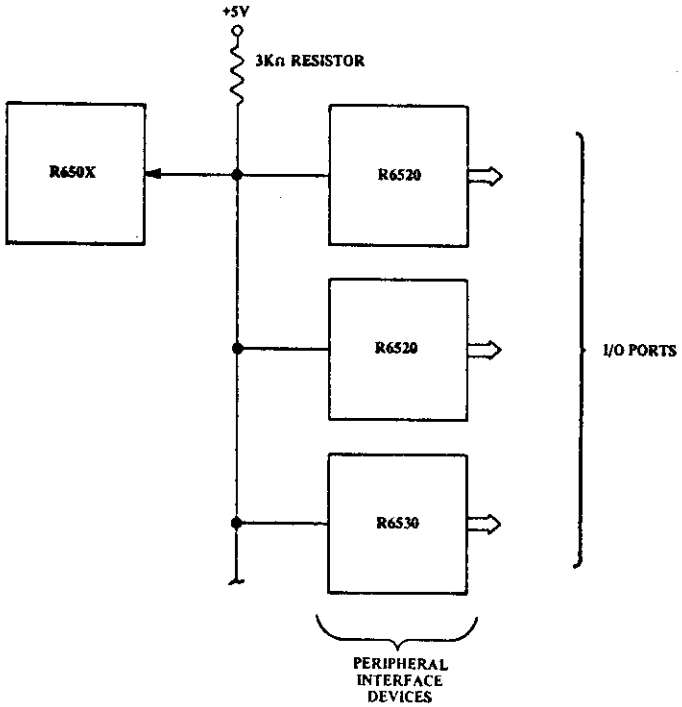
INTERRUPT SERVICING

Although a great deal has been said previously about the process of establishing interrupts and determining just what happens in response to an interrupt, it would be useful to detail the sequence which takes place when an interrupt is recognized by the processor. This will establish a basis for understanding of the details of the processor interrupt inputs.

An interrupt request is signaled by a GND (< 0.4V) signal on the interrupt request input. This interrupt will be recognized after the processor completes the instruction which it is currently executing. The next step is to store enough of the contents of the internal processor registers to assure that the processor can resume execution of the program which was interrupted. In particular, the Program Counter and the Processor Status Register are stored in a series of memory locations specified by another internal register, the Stack Pointer. As discussed in Chapter 9 of the Programming Manual, saving the contents of the Program Counter and Processor Status register uniquely defines, in memory, the state of the microprocessor at the time the interrupt occurred. The processor then goes to two fixed locations in memory to determine the address low and address high of the interrupt software.

The operation to this point is automatic and is determined by the internal processor logic. After the processor has properly set the address bus, execution of the interrupt program commences. Everything which occurs subsequently is determined by the system software.

The total interrupt software described above will consist of a complex combination of polling and interrupt servicing routines. However, unless



Interrupt Wired-OR Hardware Configuration from Peripheral Interface Devices to Microprocessor

FIGURE 1-8

a hardware prioritizing scheme is used, the actual system interconnections will not become any more complex than that shown in Figure 1-8.

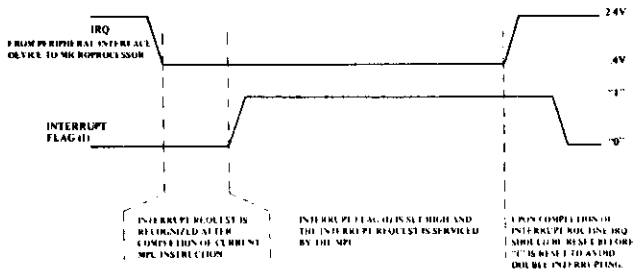
INTERRUPT REQUEST ($\overline{IRQ}$)

As stated earlier, the two interrupt lines for the microprocessor are $\overline{IRQ}$ and $\overline{NMI}$. The requirements for proper operation of the maskable Interrupt Request input ($\overline{IRQ}$) are more stringent than for the second interrupt input, $\overline{NMI}$. This is due primarily to the fact that $\overline{NMI}$ is edge-sensitive. With the $\overline{IRQ}$ input, the processor will be interrupted any time the signal on $\overline{IRQ}$ is GND (< 0.4V) and the internal Interrupt Disable flag is cleared. The Interrupt Disable flag (I) is a single bit in the internal Processor Status Register. The details of this register are described in Section 3.2 of the Programming Manual.

In the processing of interrupt request from the $\overline{IRQ}$ input, the I flag is extremely important. This is the element which assures that an interrupt will be recognized and serviced only once for each request and only when an interrupt is desired. This is described in detail below.

Figure 1-9 details the sequence of operations which should take place during the servicing of an $\overline{IRQ}$ interrupt. A positive or negative transition of the signal from the peripheral device (printer, keyboard, etc.) is detected on the edge-sensitive inputs to the peripheral interface device. If the interrupt is enabled within the peripheral interface device, the interrupt request output ($\overline{IRQ}$) on this chip will go low. The interrupt condition is latched within the peripheral interface device to allow sufficient time for the processor to poll the interrupt sources, assuring that the interrupt signal will not be cleared before the polling can be completed. This latch is reset by the processor as it executes the software associated with that interrupt. Details of this operation are described in Section 2.

The Interrupt Disable flag (I) is set automatically when the processor recognizes an interrupt. This assures that this same interrupt will not be recognized again. Resetting this flag can be performed manually with an instruction in the program or automatically with a "Return from Interrupt" instruction. It is very important that "I" not be cleared before the Interrupt input is reset. Performing the "Clear I" instruction too early in the program can cause this same interrupt to be recognized again. The processor will then proceed to service this as if it were a new interrupt.



Sequence to Service $\overline{IRQ}$

FIGURE 1-9

NON-MASKABLE INTERRUPT ($\overline{NMI}$)

The NMI input to the processor is edge-sensitive. To cause an interrupt to occur, there must be a negative transition of the signal on the $\overline{NMI}$ input. This negative transition will cause a single interrupt to occur. After servicing the interrupt, the processor will ignore this input until the $\overline{NMI}$ signal goes high (> +2.4V) and then back to ground.

The response to an $\overline{NMI}$ interrupt signal cannot be disabled within the processor. After the processor completes the instruction being executed, it will recognize the interrupt and will proceed to service the interrupt as described in the previous section. The proper discipline to employ in all interrupts is for the interrupt signal to be latched until the processor completes servicing the interrupt. This method of operation is assured if all the interrupts are connected to the interrupt inputs of the peripheral interface devices in the family.

Processing of multiple interrupts in a polled interrupt structure requires that all of the interrupts be polled before executing a "Return from Interrupt" instruction. This is necessitated by the "WIRE-OR" technique for combining the interrupts, since no knowledge exists of which line went to ground. If one of the interrupts is left unserviced, it will hold the $\overline{NMI}$ signal to ground, disabling the interrupts from all other sources since it is necessary for the $\overline{NMI}$ signal to go high (> 2.4V) and back low

again for an interrupt to occur. This is not true for the IRQ input since this latch is level-sensitive. Performing a "Return from Interrupt" before all $\overline{IRQ}$ interrupt sources are serviced will simply cause another $\overline{IRQ}$ interrupt to occur.

1.2.4 System Reset

One of the basic system control functions is the system RESET signal. Whether this signal is generated automatically by external power-on circuitry or manually from a push-button switch, the system components must obey a fixed set of rules to assure proper system operation. This is particularly true for the peripheral interface devices.

In the R650X-based systems, an assumption is made that RESET pins on all peripheral interface devices and on the processor will be held low during power-on until the supply voltages and the clocks have stabilized. This procedure assures that the peripheral pins will remain in a known state until the entire system is initialized and the processor is ready to assume control of the output lines, i.e., is ready to run the system program.

It should be mentioned that in the entire set of microcomputer chips, the contents of latches, registers, etc. are totally random after power is applied. On the peripheral output pins, random data can be disastrous. The only way to force these lines to a known condition is to apply the RESET signal. The designer can then make sure that the known condition will not cause spurious operations in the peripheral devices. The effect of RESET on the peripheral chips is discussed in the analysis of each chip.

In the processor, the single register which must be placed in a known state is the program counter. This is the register which selects the instructions to be executed. The RESET input causes the program counter to go to the first instruction in the system program. The specific details of this operation are discussed in Section 2.2.8.

There is one other very important function performed by the RESET input on the peripheral interface devices. Although the recognition of the processor interrupt signals is automatic and does not depend on software, the sequence of operations performed by the processor to totally service an interrupt is determined by the program. Until the various internal registers in the processor have been initialized, the processor is not ready to respond properly to any external interrupts. For this reason, it is important that the system RESET disable all external interrupt signals until they are enabled by the processor. The programmer can then make sure that the system has been properly initialized before the interrupts are enabled.

SECTION 2

THE MICROPROCESSOR FAMILY

2.1 FUNCTIONAL FEATURES

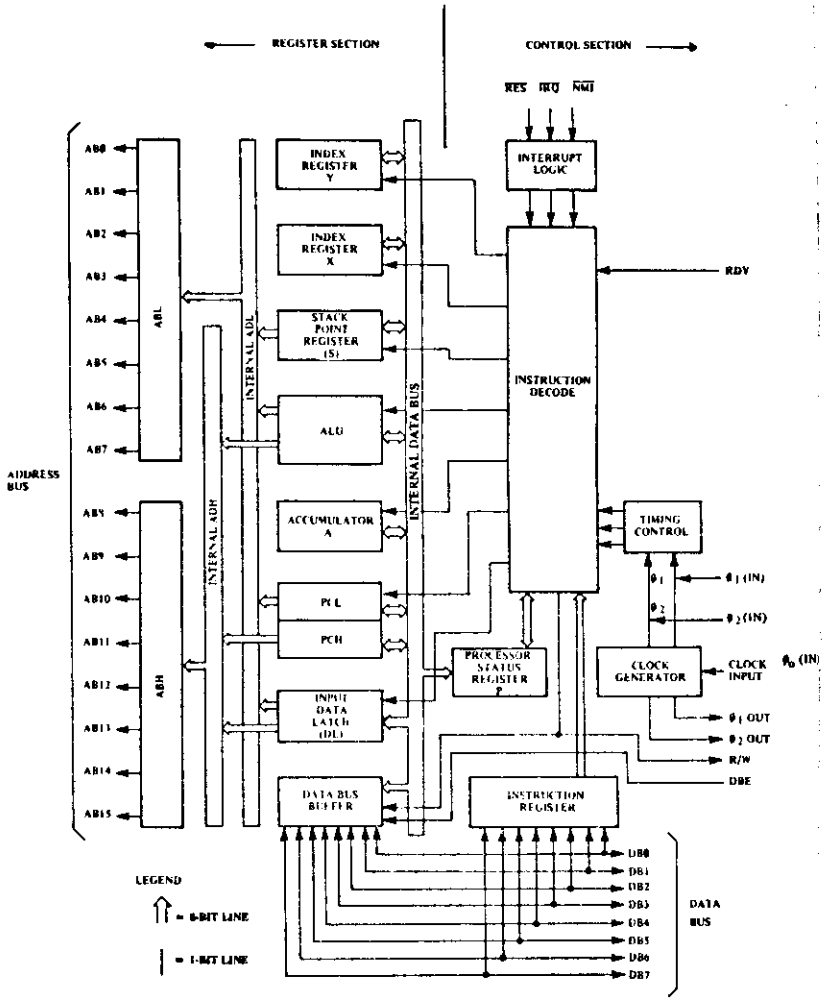
The microprocessors in the R6500 family have very similar internal architectures. A block diagram of the basic architecture is shown in Figure 2-1. This section of the manual begins with an analysis of this block diagram, discussing the function of the various registers, data paths, etc. A detailed discussion of the operation of the various pins on the chip follows.

The internal organization of the processor can be split into two sections. In general, the instructions obtained from program memory are executed by implementing a series of data transfers in one section of the chip (register section). The control lines which actually cause the data transfers to take place are generated in the other section (control section). Instructions enter the processor on the data bus, are latched into the instruction register, and are then decoded along with timing signals to generate the register control signals.

The timing control unit keeps track of the specific cycle being executed. This unit is set to "T0" for each instruction fetch cycle and is advanced at the beginning of each Phase One clock pulse. Each instruction starts in T0 and goes to T1, T2, T3, etc. for as many cycles as are required to complete execution of the instruction. Each data transfer, etc., which takes place in the register section is caused by decoding the contents of both the instruction register and the timing counter.

Additional control lines which affect the execution of the instructions are derived from the Interrupt logic and from the Processor Status register. The Interrupt logic controls the processor interface to the interrupt inputs to assure proper timing, enabling, sequencing, etc. which the processor recognizes and services.

The Processor Status register contains a set of latches which serve to control certain aspects of the processor operation, to indicate



NOTE: 1. CLOCK GENERATOR IS NOT INCLUDED ON R6512 THROUGH R6515.
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE R650X PRODUCTS

R650X Internal Architecture

FIGURE 2-1

the results of processor arithmetic and logic operations, and to indicate the status of data either generated by the processor or transferred into the processor from outside.

Since the real work of the processor is carried on in the register section of the chip, a detailed study will be made of this section. The components are:

- Data Bus Buffers
- Input Data Latch (DL)
- Program Counter (PCL, PCH)
- Accumulator (A)
- Arithmetic Logic Unit (ALU)
- Stack Pointer (S)
- Index Registers (X, Y)
- Address Bus Latches (ABL, ABH)
- Processor Status Register (P)

At 1 MHz, the data which come into the processor from the program memory, the data memory, or from peripheral devices, appear on the data bus during the last 100 ns of Phase 2. No attempt is made to actually operate on the data during this short period. Instead, it is simply transferred into the input data latch for use during the next cycle. The data latch serves to trap the data on the data bus during each Phase 2 pulse. The data can then be transferred onto one of the internal busses, and from there into one of the internal registers. For example, data being transferred from memory into the accumulator (A) will be placed on the internal data bus and will then be transferred from the internal data bus into the accumulator. If an arithmetic or logic operation is to be performed using the data from memory and the contents of the accumulator, data in the input data latch will be transferred onto the internal data bus as before. From there it will be transferred into the ALU. At the same time the contents of the accumulator will be transferred onto a bus in the register section and from there into the second input to the ALU. The results of the arithmetic or logic operation will be transferred back to the accumulator on the next cycle by transferring first onto the bus and then into the accumulator. All of these data transfers take place during the Phase 1 clock pulse.

The program counter (PCL, PCH) provides the addresses which step the processor through sequential instructions in the program. Each time the processor fetches an instruction from program memory, the contents of PCL are placed on the low-order 8 bits of the address bus and the contents of PCH are placed on the high-order 8 bits. This counter is incremented each time an instruction or data is fetched from program memory.

The accumulator is a general-purpose 8-bit register which stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

All logic and arithmetic operations take place in the ALU; this includes incrementing and decrementing of internal registers (except PCL and PCH). However, the ALU cannot store data for more than one cycle: if data are placed on the inputs to the ALU at the beginning of one cycle, the result is always gated into one of the storage registers or to external memory during the next cycle. Each bit of the ALU has two inputs. These inputs can be tied to various internal busses or to a logic zero; the ALU then generates the SUM, AND, OR, etc. function using the data on the two inputs.

The stack pointer (S) and the two index registers (X and Y) each consist of 8 simple latches. These registers store data which are to be used in calculating addresses in data memory. The specific operation of each of these is discussed in detail in the Programming Manual.

The address bus buffers (ABL, ABH) consist of a set of latches and TTL compatible drivers. These latches store the addresses which are used in accessing the peripheral devices (ROM, RAM, and I/O).

2.1.1 Functional Features of 28-Pin CPUs

Table 2-1 summarizes the functional features of the R6503 through R6507 and R6513 through R6515. The operation of each function is exactly the same as on the R6502.

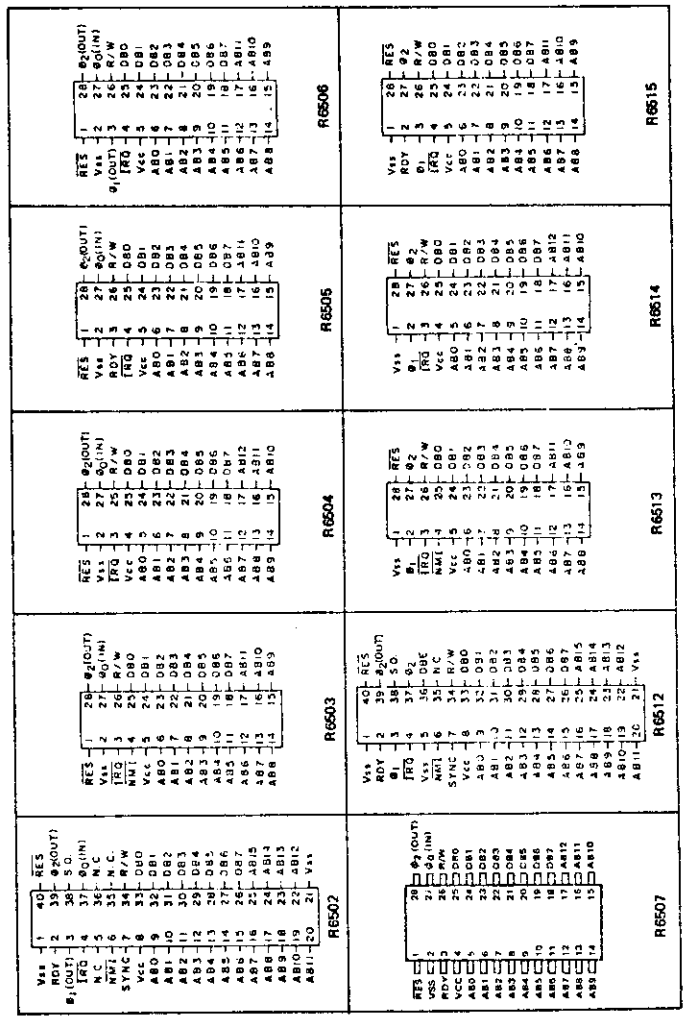
Figure 2-2 summarizes the pin designation for the eight processors, indicating the tradeoffs that exist between control signals and addressing capability due to pinout constraints. Like the R6502, five of the 28 pin microprocessors also have the on-the-chip oscillator and clock drivers.

TABLE 2-1

Functional Features of 28-Pin CPUs

Features	R6503, R6513	R6504, R6514	R6505, R6515	R6506	R6507
Addressing Capability	4096 Bytes (A00 - A11)	8192 Bytes (A00 - A12)	4096 Bytes (A00 - A11)	4096 Bytes (A00 - A11)	8192 Bytes (A00 - A12)
Interrupt Request Capability	$\overline{IRQ}$, $\overline{NMI}$	$\overline{IRQ}$	$\overline{IRQ}$	$\overline{IRQ}$	--
"Ready" Signal	--	--	RDY	--	RDY
*Timing Signals Required	Single Phase TTL Level ϕ_0 (IN), or Crystal or RC	Single Phase TTL Level ϕ_0 (IN), or Crystal or RC	Single Phase TTL Level ϕ_0 (IN), or Crystal or RC	Single Phase TTL Level ϕ_0 (IN) or Crystal or RC	Single Phase TTL Level ϕ_0 (IN), or Crystal or RC
Other Control Signals	$\overline{RES}$, R/W	$\overline{RES}$, R/W	$\overline{RES}$, RW	ϕ_1 (OUT), $\overline{RES}$, R/W	$\overline{RES}$, R/W

*6513, 6514 and 6515 are slave microprocessors requiring external ϕ_1 and ϕ_2 clock inputs



CPU Pinout Designations
FIGURE 2-2

2.2 SIGNAL LINES

Figure 2-2 summarizes the pinouts of the R6500 CPU's. These pins and their uses in microcomputer systems are discussed separately below.

2.2.1 Address Bus (AB00-AB15)

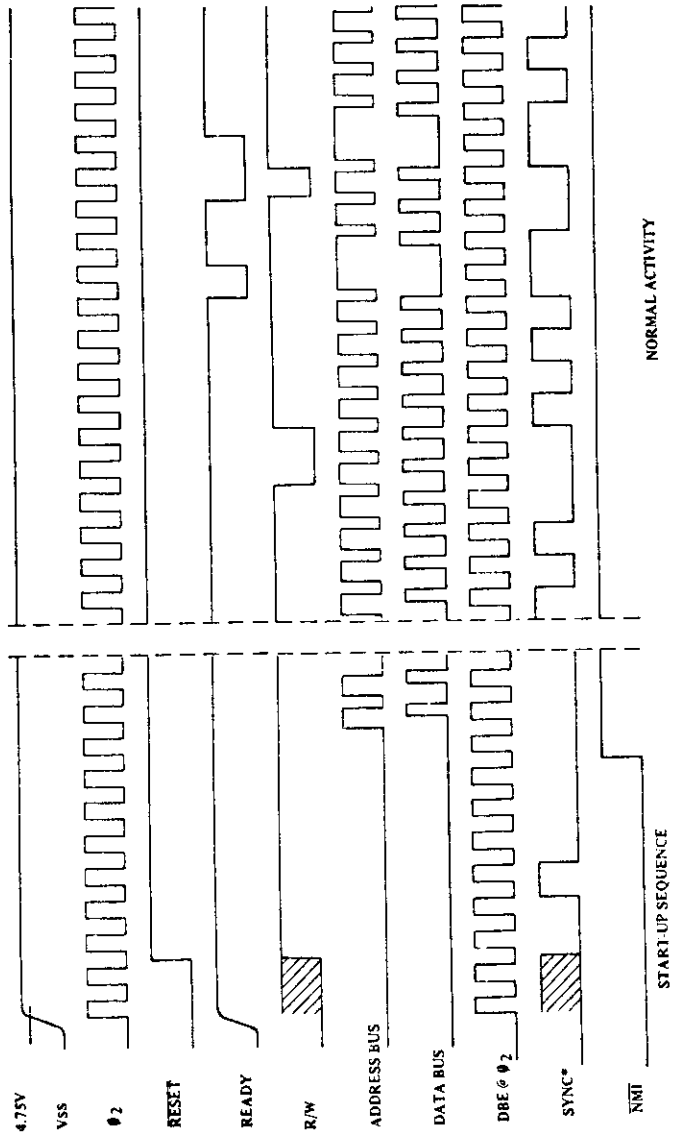
The address bus buffers on the R6500 family of microprocessors are push/pull type drivers capable of driving at least 130 pf and one standard TTL load.

The address bus will always contain known data as detailed in Appendix A. The addressing technique involves putting an address on the adress bus which is known to be either in program sequence, on the same page in program memory or at a known point in RAM. A brief study of Appendix A will acquaint the designer with the detailed operation of this bus.

The various processors differ somewhat in the number of address lines provided. In particular, the R6504, R6507 and R6514 provide 13 address lines (AB00 - AB12) and the R6503, R6505, R6506, R6513 and R6515 provide 12 address lines (AB00 - AB11). This total address space should prove to be more than sufficient for the small, cost-sensitive systems in which these devices should find their greatest application.

The specific timing of the address bus is exactly the same for all the processors. The address is valid 300 ns (at 1 MHz clock rate) into the Ø1 clock pulse and remains stable until the next Ø1 pulse: this specification will change only for processors which are specified to operate at a higher clock rate. Figure 2-3 details the relationship of address bus to other critical signals.

Because of the reduced number of address lines on the 28-pin processors, it is possible to write a program which attempts to access non-existent memory address space, i.e., the address bits 13, 14, or 15 set to logic "1." These upper address bits in the program will be ignored and the program will drop into existing address space. This assumes proper memory management when using devices of large addressing capability such that the addressed memory space will fit within the constraints of a device with smaller available memory addressing capability.



*SYNC IS AVAILABLE ON R6502 AND R6512 ONLY

R650X System Timing Diagram
FIGURE 2-3

2.2.2 Data Bus (DB0-DB7)

The processor data bus is exactly the same for the processors currently available and for the software-compatible processors which will be introduced in the near future. All instructions and data transfers between the processor and memory take place on these lines. The buffers driving the data bus lines have full "three-state" capability. This is necessitated by the fact that the lines are bidirectional.

Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the "floating" condition except when the processor is transferring data into or out of one of the support chips. All inter-chip data transfers take place during the Phase 2 clock pulse. During Phase 1 the entire data bus is "floating."

The data bus buffer is a push/pull driver capable of driving 130 pf and one standard TTL load at the rated speed. At a 1-MHz clock rate, the data on the data bus must be stable 100 ns before the end of Phase 2. This is true for transfers in either direction. Figure 2-3 details the relationship of the data bus to other signals.

2.2.3 Read/Write (R/W)

The Read/Write line allows the processor to control the direction of data transfers between the processor and the support chips. This line is high except when the processor is writing to memory or to a peripheral interface device.

All transitions on this line occur during the Phase 1 clock pulse (concurrent with the address lines). This allows complete control of the data transition which takes place during the Phase 2 clock pulse.

The R/W buffer is similar to the address buffers. They are capable of driving 130 pf and one standard TTL load at the rated speed. Again, Figure 2-3 details the relative timing of the R/W line.

2.2.4 Data Bus Enable (DBE)

On the R6512, a data bus enable signal is provided to allow external enabling of the data bus. This line is connected directly to the Phase 2 input clock signal for any normally operating system and is detailed in Figure 2-3.

The DBE signal affects only the data bus buffers. It does not affect processor timing and has no effect on the address or the R/W lines.

This input is provided primarily for use in systems which use non-R6500 devices for either the memory or the peripheral interface functions. In particular, it allows the data bus to be enabled for a period longer than the Phase 2 clock pulse for systems requiring greater processor hold time on the data bus. This application is covered in greater dedetail in Section 3.

2.2.5 Ready (RDY)

The RDY input delays execution of any cycle during which the RDY line is pulled low. This line should change during the Phase 1 clock pulse. This change is then recognized during the next Phase 2 pulse to enable or disable the execution of the current internal machine cycle. This execution normally occurs furing the next Phase 1 clock; timing is shown in Figure 2-3.

The primary purpose of the RDY line is to delay execution of a program fetch cycle until data are available from memory. This has direct application in prototype systems employing light-erasable PROMs or EAROMs. Both of these devices have relatively slow access times and require implementation of the RDY function if the processor is to operate at full speed. Without the RDY function a reduction in the frequency of the system clock would be necessary.

The RDY function will not stop the processor in a cycle in which a WRITE operation is being performed. If the RDY line goes from high to low during a WRITE cycle the processor will execute that cycle and will then stop in the next READ cycle (R/W = 1).

2.2.6 Non-Maskable Interrupt ($\overline{NMI}$)

The $\overline{NMI}$ input, when in the interrupted state, always interrupts the processor after it completes the instruction currently being executed. This interrupt is not "maskable" -- i.e., there is no way for the processor to prevent recognition of the interrupt.

The $\overline{NMI}$ input responds to a negative transition. To interrupt the processor, the $\overline{NMI}$ input must go from high (> +2.4V) to low (< +0.4V). It can then stay low for an indefinite period without affecting the processor operation and without another interrupt. The processor will

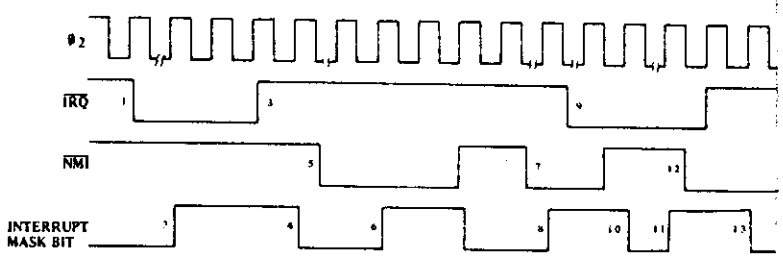
not detect another interrupt until this line goes high and then back to low. The $\overline{NMI}$ signal must be low for at least two clock cycles for the interrupt to be recognized, whereupon new program count vectors are fetched.

2.2.7 Interrupt Request ($\overline{IRQ}$)

The interrupt request ($\overline{IRQ}$) responds in much the same manner as $\overline{NMI}$. However, this function can be enabled or disabled by the interrupt inhibit bit in the processor status register. As long as the I flag (interrupt inhibit flag) is a logic 1, the signal on the $\overline{IRQ}$ pin will not affect the processor.

The $\overline{IRQ}$ pin is not edge-sensitive. Instead, the processor will be interrupted as long as the I flag is a logic "0" and the signal on the $\overline{IRQ}$ input is at GND. Because of this, the $\overline{IRQ}$ signal must be held low until it is recognized, i.e., until the processor completes the instruction currently being executed. If I is set when $\overline{IRQ}$ goes low, the interrupt will not be recognized until I is cleared through software control. To assure that the processor will not recognize the interrupt more than once, the I flag is set automatically during the last cycle before the processor begins executing the interrupt software, beginning with the fetch of program count.

The final requirement is that the interrupt input must be cleared before the I flag is reset. If there is more than one active interrupt driving these two lines (OR'ed together), the recommended procedure is to service and clear both interrupts before clearing the I flag. However, if the interrupts are cleared one-at-a-time and the I flag is reset after each, the processor will simply recognize any interrupts still active and will process them properly but more slowly because of the time required to return from one interrupt before recognizing the next. If the procedure recommended above is followed, each interrupt will be recognized and processed only once. Figure 2-4 provides several examples of interrupts, microprocessor recognition of each interrupt ($\overline{IRQ}$ and $\overline{NMI}$), and processor selection of interrupts during overlapped requests.



Examples of Interrupt Recognition by R6500
FIGURE 2-4

Each major event affecting the microprocessor is numbered in Figure 2-4, and the correspondingly numbered explanations for each are given below.

Event Number	System Activity
1.	Processor is executing from main program and $\overline{IRQ}$ goes to low state.
2.	Upon completion of current instruction, the processor recognizes the interrupt, stores the contents of PC and P onto the stack and then sets I during the fetch of the interrupt vector.
3.	After servicing the interrupt, $\overline{IRQ}$ should be reset before resetting the interrupt mask bit to avoid double interrupting.
4.	Before the processor resumes normal main program execution the interrupt mask bit will be reset low.
5.	$\overline{NMI}$ now goes low, signalling a non-maskable interrupt request.
6.	The $\overline{NMI}$ interrupt is recognized and serviced in the same manner as $\overline{IRQ}$.

Event Number	System Activity
7.	The processor has resumed normal operation when $\overline{NMI}$ again goes low requesting an interrupt.
8.	The interrupt mask bit is set high in response to the $\overline{NMI}$ request.
9.	Here $\overline{IRQ}$ has gone low to signal an interrupt request. This request is ignored since the $\overline{NMI}$ interrupt is being serviced and the interrupt mask is set.
10.	The interrupt mask bit is reset after servicing the $\overline{NMI}$ interrupt.
11.	The processor is now able to recognize the $\overline{IRQ}$ signal, which is still low, and does so by setting the interrupt mask bit.
12.	During the servicing of $\overline{IRQ}$, $\overline{NMI}$ goes from high to low. The processor then completes the current instruction and abandons the $\overline{IRQ}$ interrupt to service $\overline{NMI}$. $\overline{NMI}$ is serviced regardless of the state of the interrupt mask bit.
13.	After completing the $\overline{NMI}$ interrupt routine, the processor will resume execution of the $\overline{IRQ}$ routine, even though $\overline{IRQ}$ has subsequently gone high.

2.2.8 Reset (RES)

The $\overline{RES}$ line is used to initialize the microprocessor from a power-down condition. During the power-up time this line is held low, and writing from the microprocessor is inhibited. When the line goes high, the microprocessor will delay 6 cycles and then fetch the new program count vectors from specific locations in memory (PCL from location FFFC and PCH from location FFFD). This is the start of the user's code. It should be assumed that any time the reset line has been pulled low and then high, the internal states of the machine are unknown and all registers must be re-initialized during the restart sequence. Timing for the reset sequence is shown in Figure 2-3.

2.2.9 Synchronization Signal (SYNC)

In the R6502, a SYNC signal is provided to identify those cycles in which the processor is doing an OP CODE fetch. The SYNC line goes high

during Phase 1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the Phase 1 clock pulse in which the SYNC line went high, the processor wi-l stop in its current state. It remains in that state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single-instruction execution. This application is discussed in detail in Section 3. Figure 2-5 contains a timing diagram for this signal.

2.2.10 Set Overflow (S.O.)

This pin sets the overflow flag on a negative transition from TTL one to TTL zero. This is designed to work with a future I/O part and should not be used in normal applications unless the user has programmed for the fact the arithmetic operations also affect the overflow flag.

2.2.11 Power Lines (V_{CC}, V_{SS})

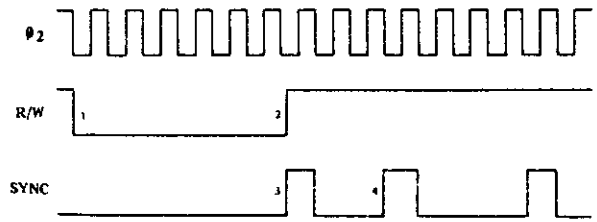
The V_{CC} and V_{SS} pins are the only power supply connections to the chip. The supply voltage is +5.0 V DC ± 5%. The absolute limit on the V_{CC} input is +7.0 V DC.

2.3 DEVICE TIMING– REQUIREMENTS AND GENERATION

The R6512 through R6515, requires a 5-volt, two-phase clock. The R6502 through R6507, however, can be used with an externally generated time base consisting of either a TTL-level single-phase clock, crystal oscillator, or RC network.

Figure 2-6 and 2-7 show the configuration for setting the frequency of oscillations with a crystal or with an RC network.

Figure 2-6 displays the crystal mode of operation in which the frequency of oscillation is set by the crystal operating in conjunction with the RC network. Figure 2-7 displays the same interconnects as in the crystal mode of time-base generation, with the crystal removed from the circuit. Values of the feedback resistor, R_F, and feedback capacitor, C_F, will be different for the crystal mode versus the RC mode. While the detail specifications for values of R_F and C_F are found in the data sheet for the R6502, clock timing can be generated by use of combinations of R_F in the range of 0 to 500K ohms and C_F in the range of 2 to 12 pf. The



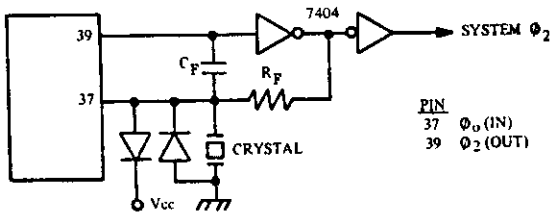
1. During a microprocessor write cycle, R/W signal low, the SYNC pulse does not occur.

2. The R/W signal goes high to signal the beginning of a microprocessor read cycle.

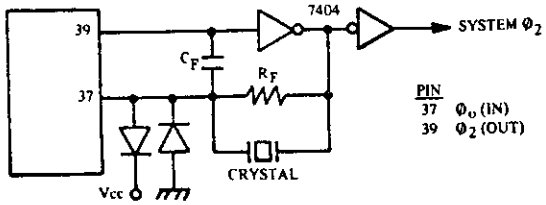
3. At the beginning of the read cycle a SYNC pulse will be be generated. This pulse will last for one cycle time. The SYNC pulse indicates that the microprocessor is reading an OP CODE from the memory field. In this case the SYNC pulse is high for one cycle as the processor reads the OP CODE.

4. The processor outputs another SYNC pulse indicating it has completed the previous instruction and is fetching another OP CODE. In this case three more cycles are needed to complete this instruction before the next SYNC pulse is generated. The SYNC pulse is aperiodic in that its generation is a function of the program and the resultant lengths of the instructions and addressing modes.

R6502 SYNC Signal
FIGURE 2-5

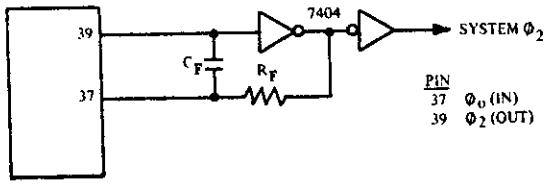


R6502 Parallel Mode Crystal-Controlled Oscillator



R6502 Series Mode Crystal-Controlled Oscillator

R6502 Time-Base Generation (Crystal-Controlled)
FIGURE 2-6



R6502 Time-Base Generator (RC Network)
FIGURE 2-7

reader is referred to the R6502 data sheet for a detailed description of the application of RC networks and crystal oscillators for generation of the time base in these modes of operation.

The R6500 bus discipline described in Section 1.2.2 is applicable wherever the oscillator is located. For data transfers to be properly carried out between the processor and the various support chips in the systems, the timing of the clocks controlling the internal processor operations must be very close to that of the Phase 2 clock out of pin 39 of the processor with no more than two TTL delays for clock buffering. It is important in systems which drive the clock generators with a TTL square wave that this input waveform not be employed to control the peripheral chips, unless care is taken to assure proper timing of the Phase 2 clock being used in these support chips.

SECTION 3

CONFIGURING THE MICROCOMPUTER SYSTEM

The first part of any microprocessor-based design effort is the microcomputer system configuration task. In fact, this probably requires more creativity from the designer than any other part of the design effort. The goal of the system configuration effort is the generation of a list of components which will make up the system, a detailed interconnect diagram, and a detailed description of the total system operation. This includes a definition of how the processor will control the peripheral devices as well as a definition of the internal operations to be performed. This does not include detailed implementation of the design such as laying out printed-circuit boards and writing programs, but does involve enough analysis of the total operation to ensure that the system will operate properly after all of the hardware and software has been assembled.

The technically based selection of components and the definition of the general operation of the system must be based on consideration of two factors:

1. System speed requirements
2. System input/output requirements

Both of these factors are interrelated. Accordingly, it will usually be necessary to define an I/O configuration, and then to verify that the processor can operate at the speed required by the peripheral devices. If there appears to be any difficulty with the I/O operation, the structure must be redefined and reanalyzed.

In addition to the speed requirements of the I/O devices, there are also general speed requirements for the internal processor operations (arithmetic operations, data manipulation, etc.). This speed requirement is usually somewhat more flexible than that associated with I/O but it should be defined along with any other system requirements. The ultimate test of system speed must wait for the generation of both the hardware and the program; however, the system requirements and capability must be analyzed very early in the system development process to ensure that no problems will arise during the last stages of the design.

3.1 INPUT/OUTPUT TECHNIQUES

3.1.1 The General-Purpose Input/Output (I/O) Port

Although the concept of the I/O port was introduced briefly in Section 1, and the operation of two R6500 system devices which provide general-purpose I/O capability has been discussed in Sections 1.5 and 1.6, little has been said about what factors must be considered when configuring I/O structure using these devices.

The general-purpose I/O port consists of eight lines, each of which can act as either an input or an output. As an input, each line can detect the state of one switch or can detect one bit of data. As an output, each line can control one light, solenoid, etc. or can provide one bit of data to a peripheral device. If this technique is used in peripheral control, the operation of each line is totally defined in the system program.

For most systems, the general-purpose interface device provides more than adequate speed and flexibility to solve the entire peripheral interface problem. Usually, cost savings can be realized because of the reduced component cost and the necessity to stock only one type of interface device. In addition, use of the general-purpose peripheral interface device allows the designer to tailor the operation of the interface device to fit the problem at hand.

The ultimate component selection must be preceded by a study of each section of the system I/O structure and a study of the overall system performance. Ultimately, the set of general-purpose and special-purpose peripheral interface devices selected for a system must be chosen to minimize total cost, while ensuring satisfactory system performance.

Processor speed is a function of two factors: (1) the number of instructions required to perform the desired operations, and (2) the percentage of processor time required to service interrupts. The typical microcomputer system may employ several interrupt signals which occur at fixed intervals. At times, these may be combined with other interrupts being generated by a peripheral device. It is important that the total service time for these interrupts does not exceed that which is allowable, and that the time available to the processor for executing the main program is sufficient to allow the system to operate at its required speed.

During the system configuration process, detailed system programs need not be generated. However, it will be necessary to write small portions of the software to verify the speed of execution and to ensure proper operation of the total system.

This chapter will discuss special techniques for the control of the various components which may be included in a microcomputer system, as well as techniques for controlling peripheral devices which are attached to the system. A discussion of programming techniques which can be used to optimize the total system performance is contained in the Programming Manual.

3.1.2 The Special-Purpose Peripheral Interface Device

The special-purpose, dedicated I/O device must also be considered in any microcomputer design. These devices are designed to completely handle a single well-defined problem -- for example, driving a particular printer, handling a particular type of communications line or driving a scanned display. These special-purpose devices are designed to totally handle their particular tasks with very little help from the processor.

The primary advantage of this type of interface device is that it requires an absolute minimum amount of attention from the processor. The major disadvantage of special purpose I/O is increased component cost. The total production volume for these devices is less than that of the more universal I/O chips and also the total chip size is usually greater.

The use of special-purpose peripheral control devices will not be discussed in this manual. Instead, a detailed study will be made of the more general problem of configuring the 8-bit bidirectional peripheral port. In addition, this chapter will cover some special techniques which can greatly enhance the power of this type of interface device.

3.1.3 Configuring the General-Purpose I/O Port

The 8-bit peripheral control port included on the R6520 and the R6530 permits each line to be programmed to act as an input or an output. This is accomplished when the processor writes a pattern of 1's and 0's into the data direction register. Writing a 1 causes the pin to become an output, and writing a 0 causes it to act as an input. Although this operation is normally performed only during system initialization, the ability to do so under program control allows some very important peripheral control techniques. An example of this is described below.

The process of configuring the general-purpose I/O port involves, first, examining the peripheral devices to analyze the various control inputs, switches, sensors, data signals, etc. which must be handled by the microprocessor to properly control the device. Each function must then be assigned to a line on the I/O port. The ultimate goal of this process is the creation of a list of I/O pins, the function of each pin, and an indication of whether each pin is to be an input or an output.

Since each line is capable of operating as an input or an output, and since there is very little to differentiate one line from any other, the actual assignment can be made fairly late in the system development cycle after consideration of software techniques and printed-circuit board layout. In fact, software considerations may be the only thing which dictates that a signal be connected to one pin or another.

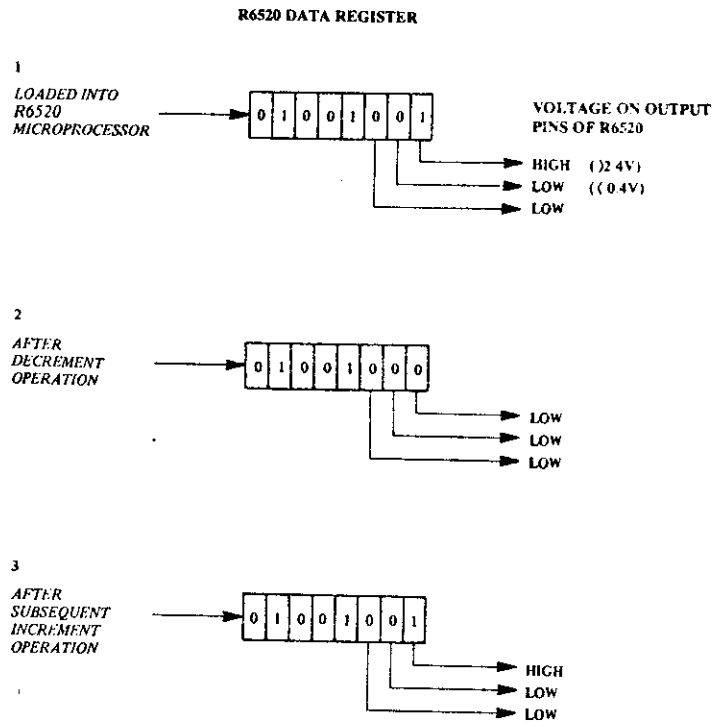
Developing a thorough understanding of the software in the R6500 systems will require a detail study of the Programming Manual. However, several operations which can be performed by the processor and which affect the assignment of inputs and outputs will be discussed briefly here.

ASSIGNMENT OF OUTPUTS

A major factor in the assignment of output pins can be the ability of the R650X processor to increment and decrement memory. Since the I/O port is treated as a location in memory, this incrementing and decrementing can be used to rapidly set and clear the low-order bit in this memory location. This is illustrated in Figure 3-1.

Note that this does not affect anything but the low-order bit if it is used properly as shown. This operation can be performed more rapidly than several other software techniques which can be employed to affect a single bit. Therefore, control of a single indicator, data line, etc. can be greatly enhanced by putting it on the low-order bit of an I/O port. This is the reason the low-order bit of both the R6530 peripheral ports (PA and PB0) provide the ability to drive transistors directly. In many applications, a simple transistor attached to one of those pins would provide very convenient control of a motor, lamp, etc.

The ability of the microprocessor to shift data in memory can be another very important factor in the assignment of outputs. Operations



Control of Low Order Bit of R6520 Output Register
FIGURE 3-1

which require sequential strobe signals can be controlled conveniently by shifting a single high (or low) signal from pin to pin under software control. The specific choice of pins can greatly enhance the ease with which this signal is controlled.

ASSIGNMENT OF INPUTS

In general, the processor deals with the input data from switches, keyboards, etc. by reading the data on the I/O port into the internal registers of the processor (usually the accumulator) and using the resulting condition of flags in the Processor Status Register to control the program which is executed. During this transfer process, the N flag in the Processor Status Register is set equal to the high-order bit (bit 7) of the word read from the I/O port. This N flag can then be used to cause the processor to execute different sections of the program (See the Programming Manual, Chapter 4, for a detailed discussion of Branching). Likewise, by performing certain instructions, the V flag in the Processor Status Register can be set equal to bit 6 on the I/O port. This flag can then be utilized to affect the program which is executed.

This operation of setting the internal flags from bits 6 and 7 of the memory word means that making these two lines inputs on an I/O port will permit very convenient testing of the condition of the switches, sensors, etc. attached to these inputs. If more than two input signals are to be attached to a port, the additional inputs should be placed on bit 5, then bit 4, and so on. The processor can then perform operations which shift the lower-order bits into bit 7 one at a time and sets the N flag equal to this bit. After each shift the N flag can be used to determine the actual program which is to be executed. (See the Programming Manual for a discussion of the Shift instructions.)

From the above example, one should conclude that the assignments which the designer makes will be very much a function of the software techniques which will be employed in controlling each line. It is very important that the designer be familiar with these techniques, and that he document the techniques which he has in mind when making the assignments. This is particularly important when the system program is to be written by someone else. Also, it is important that those persons doing the system development

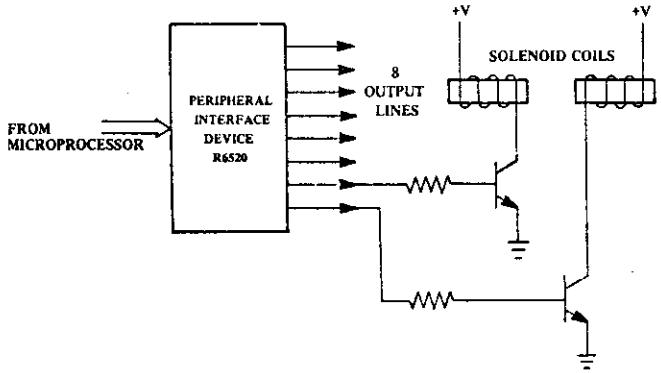
work constantly review the I/O structure to optimize the software involved as the system program is written.

3.1.4 Power-On Considerations

Section 1.2.4 discusses the operation of the system RESET function. Reference is made to the fact that this can be used to assure that all I/O lines come up in a known state when power is applied to the chip. Although this is a very important function, the designer must assure himself that this RESET state does not adversely affect the peripheral devices. This section describes some of the problems which can be encountered when the system is reset and discusses several techniques which can be used to guarantee smooth power-up operation.

The I/O lines of the R6530 and R6520 all enter the input state when the reset line goes to GND (< 0.4V). For the R6530 I/O lines, and for the Peripheral A port on the R6520, these pins will go to +5V DC (Vdd). This is due to the output structure on these pins. When these lines are in the input state, the output switch becomes an open circuit but the pull-up device continues to supply current to the pin.

Figure 3-2 shows a peripheral port which is configured to drive two solenoids. These solenoids can be controlled properly after the system is initialized; however, when the manual reset switch is activated, both I/O lines enter the input state, the transistors saturate (close) and the solenoids are activated. This can be catastrophic in most mechanical subsystems, so it is important that this potential condition be understood and prevented. Figure 3-3 shows two satisfactory solutions to this problem. The first, Figure 3-3a, requires that a "0" be written into the output line by the processor to actuate the solenoids. This ensures that the solenoids will not be powered simultaneously when the manual reset switch is pressed; however, it does introduce another potential problem. When the reset line on the peripheral interface device goes low (< 0.4V), the contents of both the Peripheral Data Register and the Data Direction register are cleared to zeros. If the Data Direction Register is set to 1's, both solenoids will immediately actuate due to the 0 stored in the Peripheral Data Register. This can be avoided completely if the system software first sets the bits



R6520 Control of Transistor Driven Solenoids
FIGURE 3-2

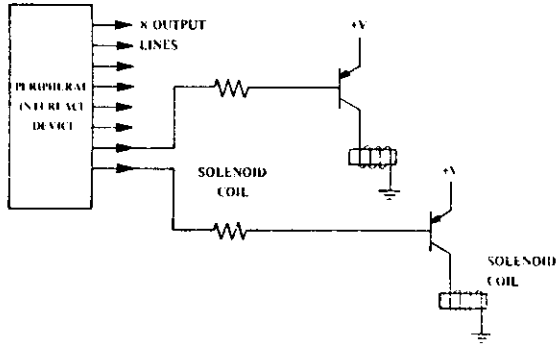
in the Peripheral Data Register to a 1 and then sets the Data Direction Register to a 1. The I/O pin will go high when the reset switch is actuated and will simply stay high through the initialization routine.

Figure 3-3b illustrates a solution which may be more applicable to a large system or a complex peripheral. In this approach, a separate output line is used to apply power to the peripheral device. The power to the entire peripheral, or to only the critical elements, is kept "off" until the entire system is initialized and is ready to run the system program.

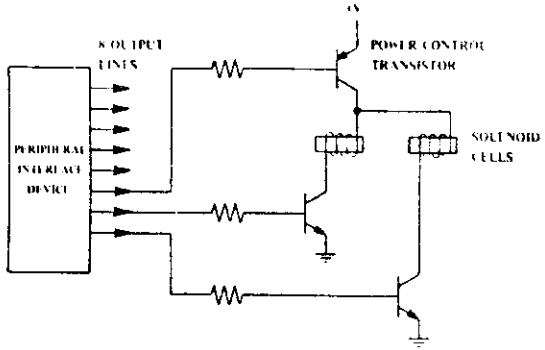
On the R6520 Peripheral B port, the I/O lines are open-circuit (high-impedance) in the input state. As a result, the configuration in Figure 3-2 will not cause the same problem on the R6520 Peripheral B port as would be expected on the R6530. In the input state, the I/O pin is incapable of sourcing any more than a few microamps.

However, if one were to use a solenoid driver as shown in Figure 3-4, the TTL input structure on the drivers would interpret the high-impedance state as a logic 1 and would actuate the solenoids; both the solutions in Figure 3-3 would be satisfactory in this case. However, the transistors are connected to the TTL buffer. In addition, the extra output shown in Figure 3-3b, controlling power to the peripheral device, could actually be utilized to enable the solenoid drivers if an enable input is available to these devices. This configuration is illustrated in Figure 2.5.

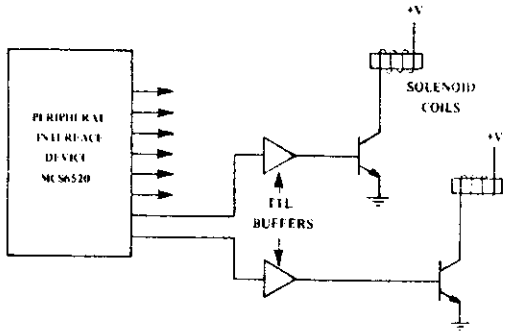
R6520 Control of PNP Transistor Driving Solenoid Coil
FIGURE 3-3a

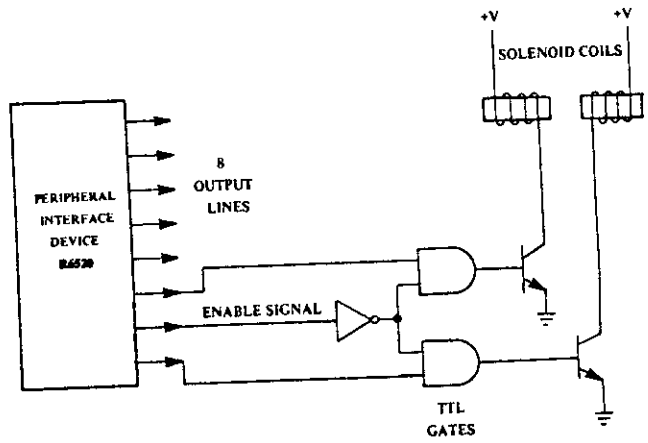


R6520 Controlling Both Power and Drivers of Solenoid Cell
FIGURE 3-3b



R6520 Driving TTL Buffers
FIGURE 3-4





R6520 Controlling Solenoids with Enable Signal and TTL Interface
FIGURE 3-5

3.1.5 Handshaking

The R6520 provides both interrupt control and data transfer control capability. The technique for controlling the transfer of data between the processor and a peripheral device is referred to as "handshaking." In this procedure, each device (the processor or peripheral) is capable of signalling the other that its operation is complete. The sequence differs somewhat for transfers into or out of the processor, so they will be discussed separately below.

HANDSHAKING ON DATA TRANSFERS FROM THE PROCESSOR

The transfer of data out of the processor into a peripheral device is performed by first writing the data into the data register within the R6520. These data then appear on the peripheral output lines where they can be read by the peripheral device for storage, display, etc.

Control of this data-transfer by handshaking requires first that the processor signal the peripheral device that data are available on the I/O port. The peripheral device then reads these data and signals to the processor that the data have been taken and that new data can be made available. The processor then makes new data available and the cycle is repeated.

As described in Section 1, the Peripheral B Interface Port on the R6520 is designed to perform handshaking on WRITE operations. The CB2 peripheral control line can be programmed to act as an output which goes low each time the processor writes data onto the Peripheral B I/O port. This is the signal which tells the peripheral device that data is available on these output lines.

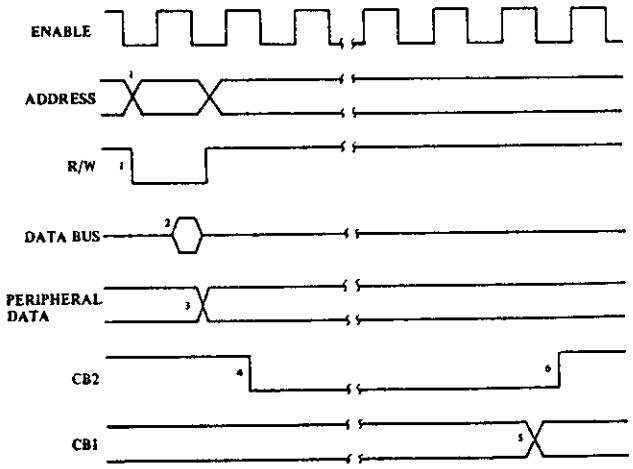
The CB2 output line will stay low until the peripheral device signals the processor that the data is taken. This is accomplished by interrupting the processor through the CB1 interrupt input.

The sequence which takes place during the "WRITE" handshaking operation described above is shown in Figure 3-6.

HANDSHAKING ON DATA TRANSFERS INTO THE PROCESSOR

The Peripheral A I/O port on the R6520 is designed to handshake on data transfers from the peripheral device into the processor. In this sequence, the peripheral device must signal the processor that data are available and the processor must signal back that data was taken. This is basically the same sequence as that performed in the previous operation. The CA1 interrupt input is used to interrupt the processor to indicate that there are data available on the Peripheral A I/O port. The peripheral device must then hold the data there until the processor reads them into its internal registers. When the processor reads the Peripheral A I/O port, the CA2 peripheral control line goes low to signal to the peripheral device that the data have been taken and new data can be made available. This entire sequence is shown on Figure 3-7.

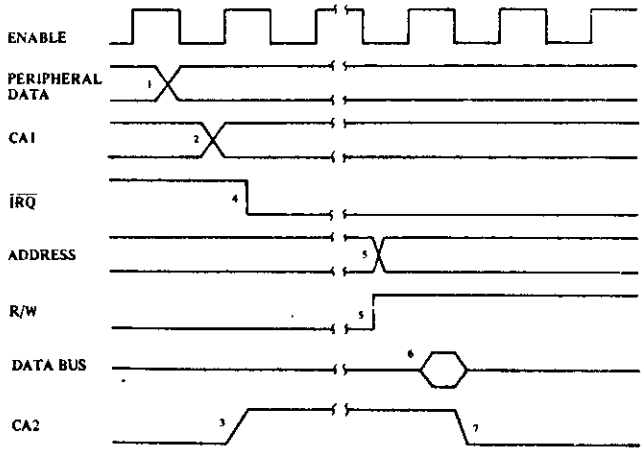
The handshaking operations described above can be an extremely powerful technique for interfacing data storage devices or, in general, any device which must transfer blocks of data and which has a variable response time. If the processor cannot predict the speed with which the



1. Processor puts out address of peripheral device and changes R/W signal to write enable (low).
2. During Phase 2 processor puts out data on Data Bus.
3. Data from the processor is accepted by the R6520 on the falling edge of the enable clock.
4. Peripheral Interface device now begins the handshake by signaling the peripheral device that data are available to read on the output port.
5. When the external peripheral device reads the data on the output port it will respond by a change in CB1.
6. The change in CB1 is followed by a positive transition of CB2 signalling the processor that data were accepted.

Write Handshake Sequence

FIGURE 3-6



1. New data are put out by peripheral device.
2. The peripheral interface device is signaled by CA1 that the new data are ready to read at the input port.
3. CA2 is put into the high state.
4. The processor is signalled that new data are ready to be read by a low level on the $\overline{IRQ}$ line.
5. The processor begins servicing the Interrupt request, and during the routine the processor will put out the read signal and the Address of the Peripheral Interface device.
6. The Peripheral interface will transfer the new data from the peripheral device to the microprocessor through the data bus.
7. When data have been transferred, the peripheral device will be signaled by CA2 going low.

Read Handshake Sequence

FIGURE 3-7

peripheral takes data, for instance, it must rely on the peripheral to signal that it has done so.

Initiating the data-transfer sequence is usually accomplished through a set of I/O lines separate from the port which is transferring the data. However, once the sequence is under way, the processor must deal with the peripheral device only when an interrupt has occurred. This allows the processor to execute the primary system program while still servicing these peripheral devices.

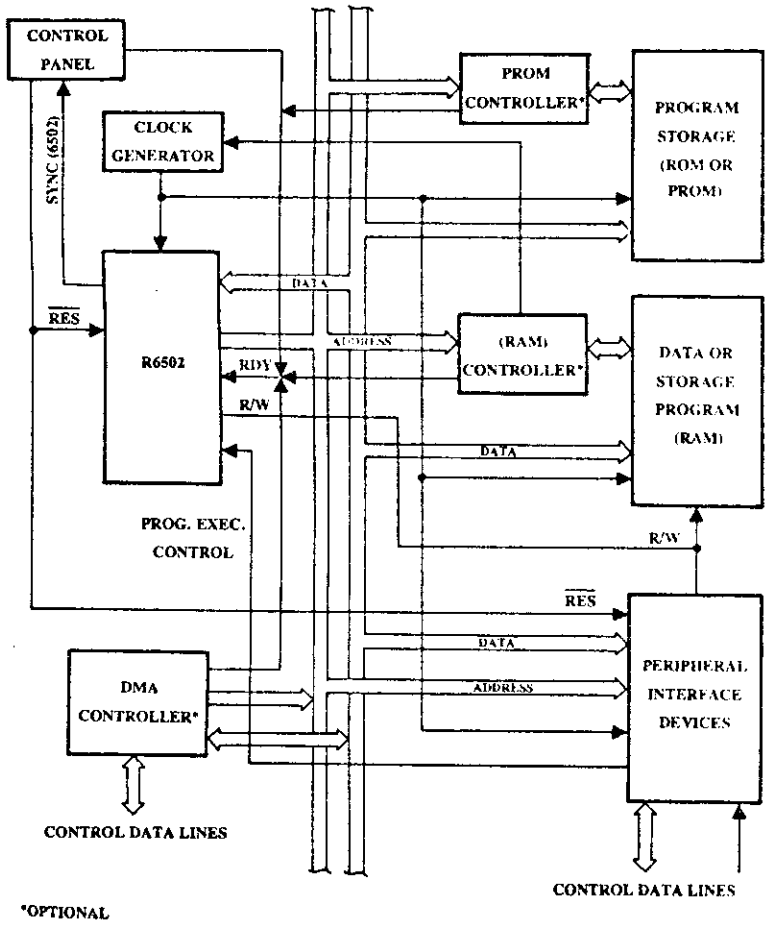
3.2 THE MICROPROCESSOR/SUPPORT CHIPS INTERFACE

The system block diagram (Figure 3-8) shows the basic data paths which allow the R6500 system to operate. Data Bus, Address Bus, R/W signal, etc. are shown as simple connections between the various chips in the system. These data paths will exist in any system, no matter how complex. Nevertheless each element of the microprocessor interface must be examined to ensure that each chip is properly driven with signals which meet all specifications for the device, that the inter-chip timing is proper, and that the overall system is operating as required.

3.2.1 Assigning Addresses in the R6500 System

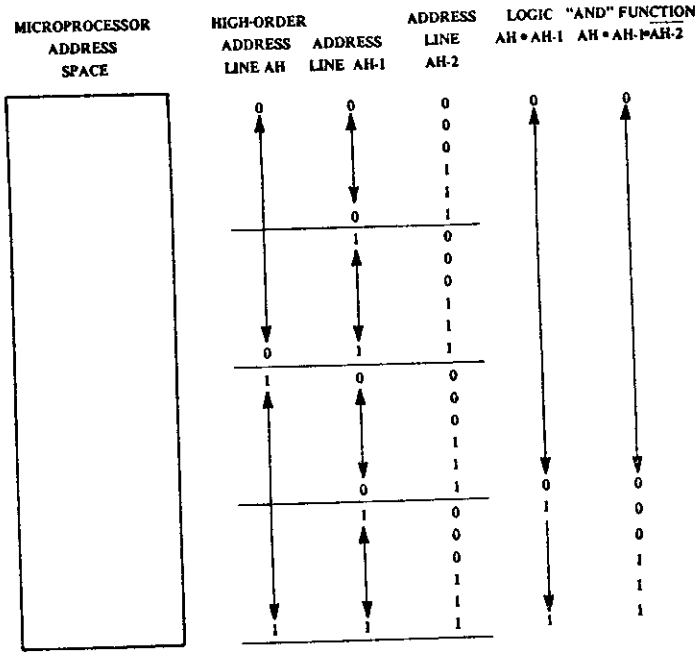
The only method which the microprocessor has for selecting between the various RAMs, ROMs, etc. in a system is through the address output lines. For this reason, the designer must use these lines very carefully to achieve minimum system cost and to ensure satisfactory system performance.

Before looking at how the address lines can be configured to minimize total system cost or program execution time, the designer should understand how the binary value associated with each address line is related to the total address space available to the microprocessor and how the AND function of various address lines can be employed to select large blocks of addresses. Figure 3-9 illustrates the state of the three high-order address lines for the entire address space available to the R650X. Note that the highest-order address line is a logic 1 for exactly half of the available address. The AND function of the two highest-order address lines is a logic 1 for one-fourth of the available addresses, and so forth. Figure 3-9 also illustrates several AND functions derived from the three highest-order address lines; each is true for a different block of the available addresses.



Organization of Microcomputer System

FIGURE 3-8



Example of "AND" Function Using High-Order Address Lines
FIGURE 3-9

Generation of the AND function of various high-order address lines is extremely important because of the chip select techniques employed on the processor support chips. As described in Section 5.1.4, the R6520 has three chip-select lines. The entire chip is selected for reading or writing data when CS1 and CS2 are high (> 2.4V) and CS3 is low (< 0.4V). Selection of the address lines which enable the various chips in the system is a very basic but very important part of the system configuration task.

It is important to note here that very few microprocessor-based systems actually require that the processors be able to access a full 65,536 words. In fact, most systems can be programmed in less than 2,000 words for program and data memory. The full address space is made available primarily because it permits the configuration of systems with an absolute minimum of separate decoding chips between the processor and the support chips. It is possible to assign any block of address to each type of chip (RAM, ROM, peripheral interface chips, etc.) in the system. However, each of the assigned addresses must be mutually exclusive. Only one of the support chips should be selected for every address used in the system program.

ROM ADDRESS ASSIGNMENT

The assignment of ROM addresses is dictated by the fact that the interrupt and RESET vectors must be located in the six high-order words in memory. These are fixed vectors and must be stored permanently in these locations. For this reason, the program memory (usually ROM) is usually assigned the high-order addresses. In fact, the recommended procedure is to use A15 (A12 for R6504 and R6507 and A11 for R6503, R6505 and R6506) to select program ROM.

RAM ADDRESS ASSIGNMENT

There are several factors which determine the location of the RAM in an R650X-based system. Data stored in memory under control of the internal processor Stack Pointer will always go into Page One (ADH = 01). Also, the entire set of Page Zero addressing modes relies on there being data storage RAM in Page Zero. For this reason, the RAM in a R650X-based system should be placed in the low-order addresses in memory.

With the RAM in low-order memory and the ROM in high-order memory, the peripheral interface devices must go somewhere in between. This is

accomplished in Figure 2.10 by using A15 · A14 to select ROMs, $\overline{A15}$ to select RAM, and A15 · $\overline{A14}$ to select all peripheral interface devices. This allows differentiation between the types of support chips. The addressing structure can be completed by allowing for selection of each chip in the groups.

The addresses which select the various registers, peripheral ports, etc. within the peripheral interface devices that are normally employed will not be sequential. For this reason, it is usually recommended that the technique shown in Figure 3-10 be employed to differentiate between the peripheral interface chips. This permits selection of 12 devices with no decoding in a R6502-based system, up to nine R6520 devices in a R6504 or R6507 based system, and up to eight devices in a R6503, R6505 or R6506-based system.

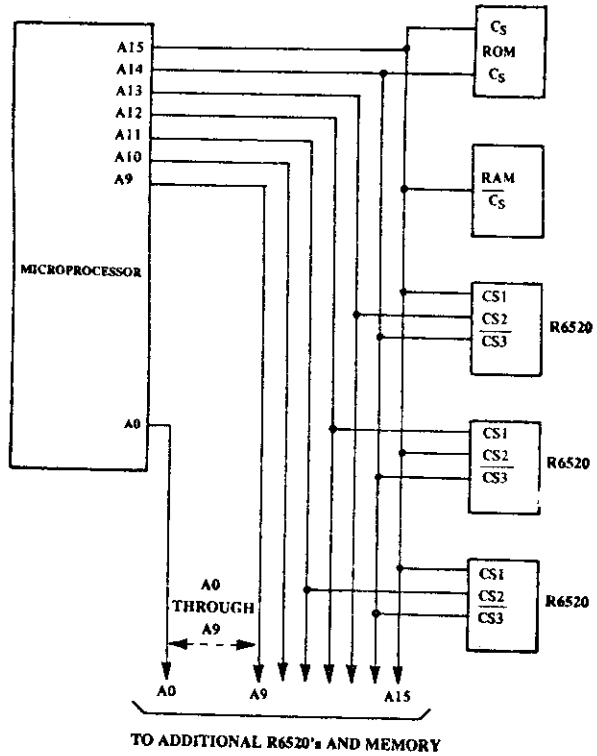
ADDITIONAL ADDRESS ASSIGNMENT TECHNIQUES

In many systems, the techniques illustrated above may not represent the best solution to the system problem. This is particularly true if program execution speed is a primary consideration. The time required to access the peripheral devices can be reduced by putting these devices in Page Zero. The entire set of Page Zero addressing modes can then be used to access these devices. In addition, the polling of the R6520 control registers during interrupt servicing can be facilitated greatly by putting the control registers in sequential addresses. These registers can then be accessed, making use of the Page Zero, Indexed addressing mode described in the Programming Manual. The address interconnect which allows this is shown in Figure 3-11. Note that this implementation requires external address decoding chips, but, for the system requiring it, this incremental cost will result in high operating speeds.

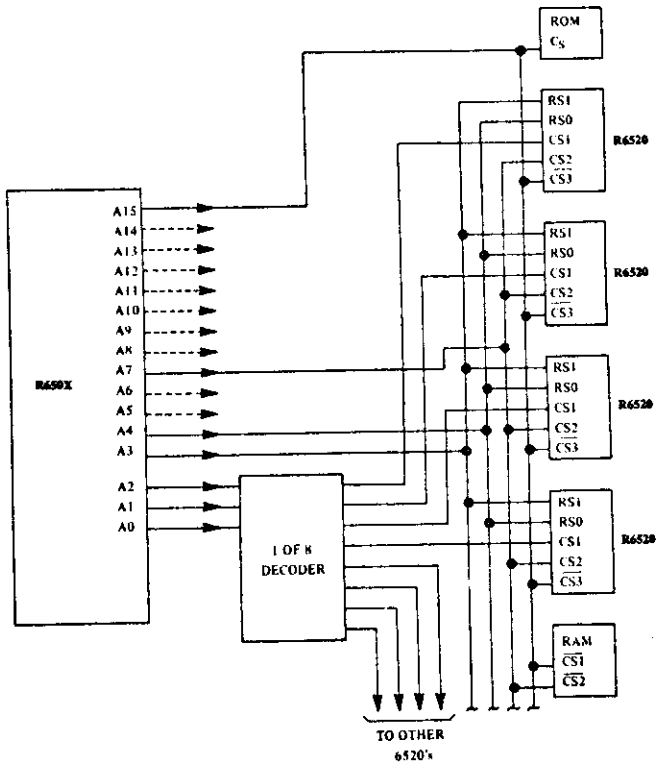
The system designer must become familiar with the addressing lines and their effect on the address space available to the processor. Even more importantly, there is a significant relationship between software and hardware in microprocessor systems and a full understanding of both can facilitate optimization of the trade-off between speed and cost for the system under design.

3.2.2 Interrupts

The basic concept of interrupts is introduced in Section 1.2.3 of this manual. However, little is said there about the hardware and software



Typical Address Assignments
FIGURE 3-10



Page Zero Chip Select Addressing Scheme
FIGURE 3-11

techniques which are required to assure proper implementation of the interrupt system. This section is designed to introduce the designer to the details of interrupts and interrupt servicing techniques.

INTERRUPT PRIORITIZING

Chapter 1 makes reference to various techniques for hardware prioritizing of interrupts to allow more rapid servicing of interrupts. The goal of this hardware is to allow the processor to go directly to the program which services the highest-priority active interrupt without taking the time to poll each interrupting device.

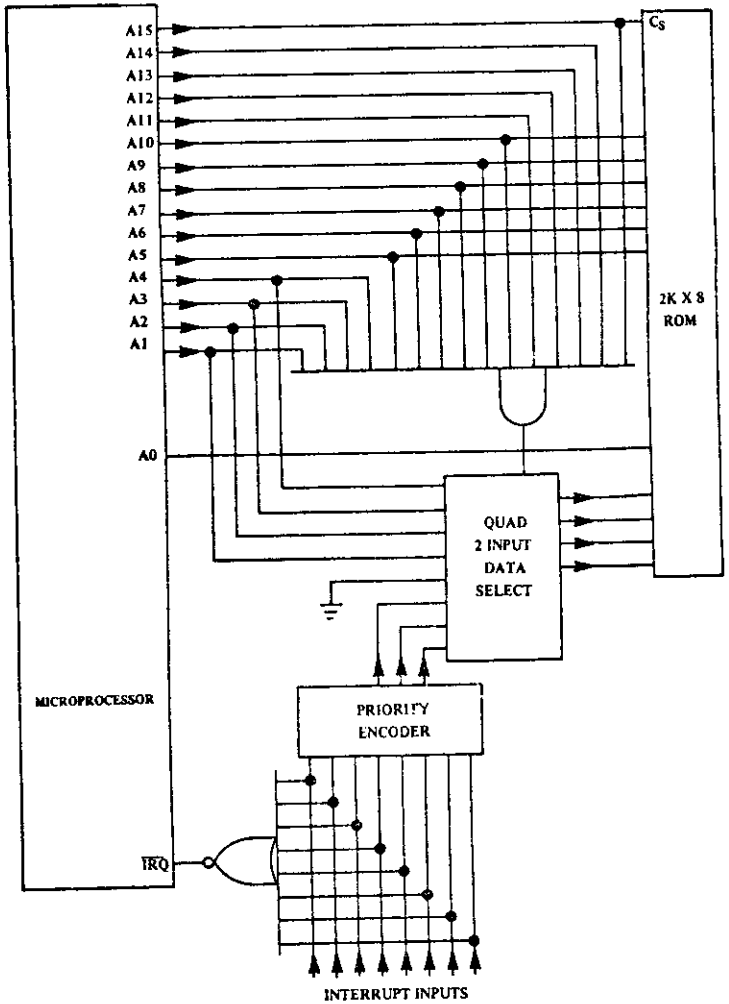
All hardware prioritizing techniques are based on the "priority encoder" shown in Figure 3-12. This device has eight inputs which are assigned a priority level from one to eight and generates a three-bit binary code corresponding to the highest-priority active input signal.

The generation of this three-bit code is in reality a trivial task for the designer. However, relating this code to the address of the corresponding interrupt service routine is much more difficult and represents an opportunity for creativity on the part of the designer. Several solutions will be illustrated here to demonstrate what can be done. These are certainly not assumed to be the only solutions. Each system must be considered separately to assure that the implementation chosen is as close to optimum as possible.

EXAMPLE 1: SELECTING THE INTERRUPT VECTOR

The final step of interrupt response within the processor is the fetching of an interrupt vector from two fixed addresses in memory. The interrupt vector located in these fixed addresses identifies the address of the software which the processor executes to poll the interrupting devices. Instead of pointing to the polling routine, it would be much faster to go directly to the software which actually services the interrupt. This requires a unique vector for each interrupt.

The technique illustrated in Figure 3-12 assumes that the interrupt vectors are located in ROM at addresses below that normally assigned to the interrupt vector. The decoder detects the fact that the processor is reading FFFE or FFFF. At this time the address inputs AD1, AD2 and AD3 into the ROM are driven from the priority encoder. Instead of accessing FFFE or FFFF, the



Selecting the Interrupt Vector

FIGURE 3-12

interrupt vector will come from two addresses selected by the priority encoder. The actual hardware involved is quite simple and the interrupt response time is an absolute minimum.

EXAMPLE 2: USING THE PROCESSOR SOFTWARE POWER

These several solutions to the vectored interrupt problem take advantage of certain instructions which can be performed by the processor. The first of these employs an instruction called the "Jump Indirect." This instruction causes the processor to begin executing the program located at that address contained in two sequential memory locations.

As in Example 1, the three-bit output from the priority encoder becomes part of the address of the interrupt software. If the output of the priority encoder is connected to the inputs of a peripheral interface device, the processor can then perform a Jump Indirect operation using the address on the two peripheral I/O ports. This is illustrated in Figure 2.13.

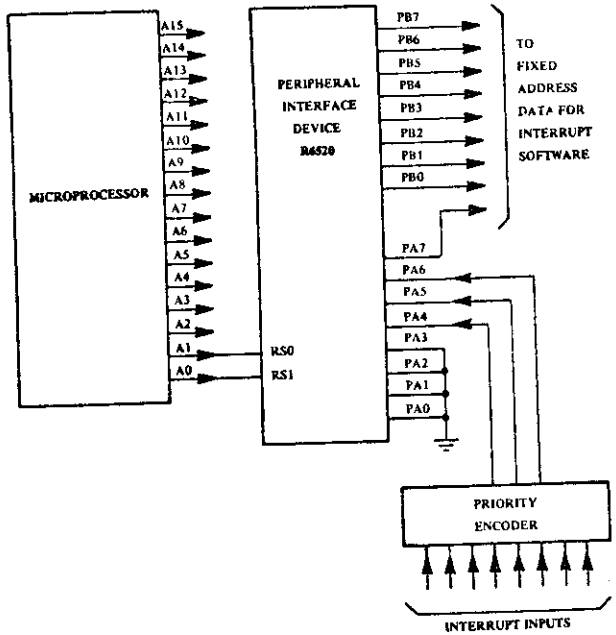
Another solution which takes advantage of the processor software is shown in Figure 3-14. Once again, the output of the priority encoder is connected to the inputs of a peripheral I/O port. However, in this approach, the priority encoder is connected to the low-order bits and the other bits can serve as control or input lines for other functions.

In this method, the three bits from the priority encoder will become part of an address established in memory. This address will then be used in a Jump Indirect instruction as before. This operation is detailed in Figure 3-15.

3.2.3 Memory Interface Control Using RDY

The ability to stop the microprocessor can be extremely important when using memory devices that are not directly compatible with the R650X family.

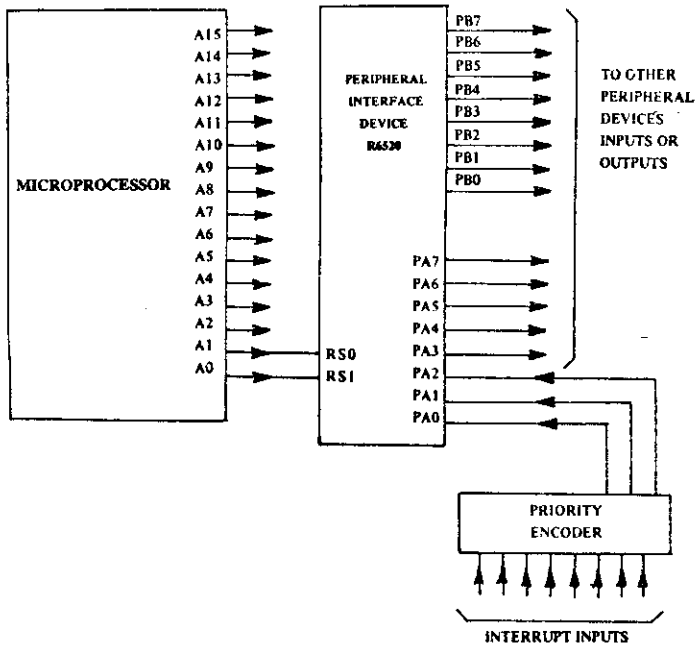
The RDY line can be used to stop the processor in any "non-write" cycle -- i.e., any cycle in which the processor is not attempting to write data into memory. The processor can be stopped for any number of clock cycles -- from one cycle for interfacing with slow memories to many cycles for DMA applications and for single cycle execution.



NOTE: CONNECTING THE ADDRESS LINES AS SHOWN PUTS THE TWO R6520 I/O PORTS IN SEQUENTIAL ADDRESSES.

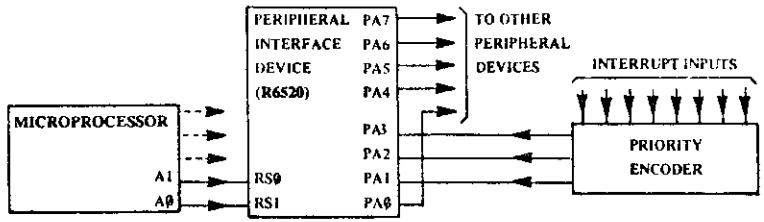
Using R6520 for Jump Indirect Interrupt Routines

FIGURE 3-13



Priority Encoder Connected to Low-Order Bits of R6520

FIGURE 3-14 a



Priority Encoder to Peripheral Interface Scheme

FIGURE 3-14 b

Priority Encoder Connection Schemes

FIGURE 3.14

```
INTVEC --→  PHA                    Receive Interrupt Vector
            TXA
            PHA
            LDA    IPA AO          Read PIA Port
            AND    #0E             Clear PIA
            TAX                    Transfer Acc. to X index reg.
            LDA    VEC TAB, X      Load Acc. from Interrupt Vector
                                   Table stored in memory
            STA    JMP1            Set Low-Order Address Byte
                                   of Interrupt Vector
            INX                    Increment X Index Register
            LDA    VEC TAB, X      Load Acc. from Interrupt Vector
                                   Table
            STA    JMP1+1          Set high-order Address Byte
                                   of Interrupt Vector
            JMP    (JMP1)          Go to Interrupt Service
                                   Software
```

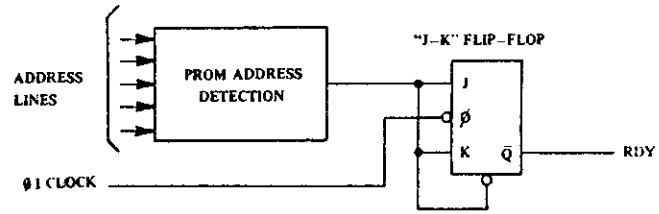
Software Program to Implement Interrupt from above Hardware Configuration

FIGURE 3-15

INTERFACING SLOW PROMS

One of the principal applications of RDY is in the control of light-erasable PROMs or EAROMs. These devices generally have longer access times than that required by the microprocessor when operation at 1 MHz clock frequency and are incapable of making data available on the data bus within 100 nanoseconds of the end of the Phase 2 clock pulse. The Phase 2 clock pulse is used to latch data or instructions on the data bus; therefore, if the data are not available at the correct time, the processor must be held up for one full cycle. The instruction will then be latched on the following Phase 2 pulse. Execution of the instruction will then proceed during the next cycle. Suggested logic for performing this function is shown in Figure 3-16.

Note that the data present on the data bus during the Phase 2 clock pulse after RDY goes high are the data that will be used in the instruction execution which takes place during the following cycle.



Interfacing Scheme for Slow PROM's

FIGURE 3-16

DIRECT MEMORY ADDRESS (DMA) TECHNIQUES

Transfer of data from peripheral storage devices into the microcomputer data memory (RAM) can normally be handled one byte at a time under control of the microprocessor. However, in large data terminals, control systems, etc. the primary data storage device may be a high-speed tape or disk. In systems such as these, the data transfer from the storage device into memory must be performed at speeds greater than the processor can handle. The control of the transfer must be performed outside the processor in a separate controller, and the peripheral device must gain direct access to the system RAM.

Direct Memory Access requires primarily that the processor have no need to access the memory involved. This is generally ensured by stopping the processor completely. The DMA controller must then gain access to the R/W line and both the address and data busses on the memory unit.

Provision for stopping the processor is available on the R6502, R6505 and R6507. This is accomplished by pulling the RDY line on the processor to GND (< 0.4V). The processor will stop in the first non-write cycle with the data bus in the high-impedance state. After the processor has stopped, the DMA controller must provide the address and data for the memory and must control R/W if data are being transferred into memory.

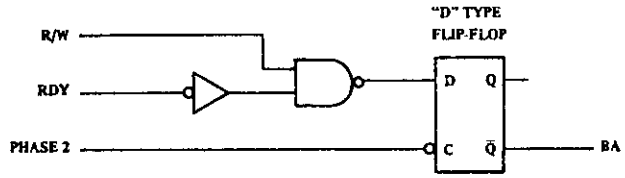
Providing addresses for the memories can be accomplished by gating addresses from either the DMA controller or the microprocessor into the memories. This can be accomplished very easily with a Quad 2-input data selector. During the DMA operation, the addresses fed to the memories are those generated by the DMA controller. After the DMA operation is complete, the input-select signal to the data selector is inverted, and the addresses generated by the processor once again determine which memory word is being accessed. The R/W line to the memories can be controlled in the same way as the address lines.

The data bus must be controlled in a somewhat different manner. This is necessitated by the fact that these lines are "bidirectional," with the data bus pins on the processor and the support chips serving for both input and output. The output buffers in each of these chips are capable of entering a high-impedance state to allow any of the devices to drive the bus during data and instruction transfers. For this reason, a bidirectional, "three-state" bus extender is required to interface the DMA controller to the system data bus. The logic necessary to provide full address bus and data bus control for DMA applications is shown in Figure 3-17.

The R6502, R6503, R6504, R6505, and R6507 do not make provision for the Bus Available signal. However, these processors still stop in the first non-write cycle. For this reason, the logic shown in Figure 3-17 should be used to generate a Bus Available signal for the DMA controller.

CONTROL OF DYNAMIC RAMS IN THE R6500 SYSTEM

For systems which must contain a large quantity of Read/Write memory (RAM), the 4096-bit dynamic RAMs can provide the required storage with a minimum number of parts. However, there is one major drawback to these devices -- they must be refreshed periodically. For most devices currently available, this refresh period is about 2 milliseconds for the entire chip. Refreshing the entire chip requires 32 Read operations which can be performed all at once every 2 milliseconds, or performed one-at-a-time approximately every 64 microseconds.



Logic Used to Generate Bus Available Signal for DMA Applications
FIGURE 3-17

Unless a separate controller is used to perform this refresh operation, the use of dynamic memories can be very detrimental to system performance.

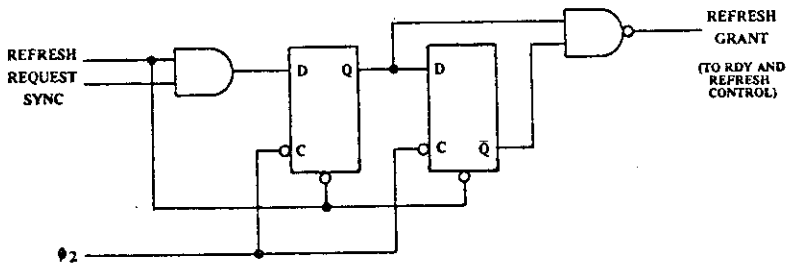
As with any Direct Memory Access, the processor must be stopped to assure that the processor and the DMA controller are not attempting to access the memories concurrently. The RDY input provides this capability. A counter operating directly from the system clock will provide a very convenient refresh signal. Each time the counter goes through a count of 63, a "refresh request" pulse is generated. The actual memory refresh operation must take place during a Read operation with the processor stopped for 1 cycle. Determining when the processor has stopped presents exactly the same problem as in DMA operations. The controller must pull the RDY line low and must then examine the R/W line to determine when the processor is in a Read cycle.

The specific operation performed during the refresh cycle is a function of the devices being used. However, it should be noted that the time available for refreshing the memory is "N - 1/2" cycles, where N is the number of cycles that the processor is stopped. Control of the memory address lines must be returned to the processor at the beginning of Phase 1 if the memories are to have a full cycle to make valid data available on the data bus. This leaves one-half cycle available to perform

the refresh operation if the processor is stopped for one cycle. A full 1-1/2 cycles can be made available by stopping the processor for two cycles. This latter implementation is more compatible with most dynamic RAMs currently available.

As described above, a primary problem in the implementation of dynamic RAM systems is related to knowing when the processor has stopped. A full one-half cycle is required in the implementations described above. The R6502, however, provides a signal -- the SYNC signal -- which can be utilized to predict that the processor will stop in the very next cycle. It is impossible for a Write operation to immediately follow an instruction fetch cycle. This allows the memory refresh controller to assume control of the address lines at the beginning of that cycle instead of after the trailing edge of Phase 1.

The RDY line is pulled low on Phase 1, and the processor is guaranteed to stop. Control of the address lines is returned to the processor on the next Phase 1 and RDY is set high at the same time. The result is the refresh logic has a full cycle to refresh the memories and the processor loss only one cycle of execution time. A suggested configuration for this control logic is illustrated in Figure 3-18.



Control Logic for Refresh Signal for Dynamic RAMS
FIGURE 3-18

3.3 ADDITIONAL SYSTEM CONSIDERATIONS

After the basic system configuration is complete, extensive breadboarding and testing are usually required before the design is finalized. However, this breadboarding and evaluation must be preceded by a complete evaluation of the cost and performance of the proposed design to guarantee that the various goals of the project will be met.

The first step in evaluating the design is to estimate the amount of ROM and RAM that will be required, as well as the number and type of interface devices required to control the peripherals

3.3.1 Peripheral Interface Devices

The number and type of peripheral devices can generally be estimated very accurately. However, it is important to keep in mind that these estimates must be subject to review after a full analysis of system performance is completed. The designer may find it necessary to employ a special-purpose interface part or to redesign the I/O structure if the evaluation of system performance reveals that the system cannot operate at the required speed. Use of special-purpose peripheral interface parts will reduce the number of tasks which must be handled by the processor and consequently can increase the overall system speed, but this generally involves additional component cost.

Similarly, the use of a fully vectored interrupt can lead to increased performance at increased cost. The goal of any design program must be to meet all the system performance at the minimum possible cost.

After the various peripheral devices in the system have been evaluated to determine the number of inputs and outputs required, the total required by all peripherals can be divided by 16 to determine the number of devices required. This is a good first approximation which will be re-evaluated as the system development progresses.

3.3.2 RAM

The evaluation of the amount of RAM required by the system is a somewhat more difficult problem than estimation of peripheral devices. This is due primarily to the fact that much of the RAM is required by the system software as working storage, such as storage of immediate results in

arithmetic operations. Since the system program will probably not be written when these estimates are first attempted, the probability of error in this portion of the estimate may be fairly high.

In addition to working storage, the RAM must provide storage for:

1. The "stack" (described in the Programming Manual)
2. Peripheral input data storage
3. Peripheral output data storage

Items 2 and 3 above can be evaluated quite accurately, since a detailed analysis of the peripheral devices has usually been completed when these estimates are first attempted. In general, a block of RAM must be made available for each peripheral device. The amount of RAM required for each is a function of the type of peripheral device being interfaced and just how the device is to be controlled.

The amount of RAM required by the stack is a function of both the interrupt structure and the system software. As a result, an estimate of this requirement must be based on the system programmer's best estimates of his requirements. This should be combined with an estimate of the required working storage and the peripheral data storage requirements to obtain an estimate of the total system RAM.

3.3.3 ROM

The amount of ROM required in a system cannot be determined accurately until the system program is completed. However, by partitioning the system program into definable pieces, an estimate can be made of each task and the total can be obtained of the ROM required by each section.

Most programs consist of easily defined sections such as the software for each peripheral device, arithmetic routines, etc. These are the pieces which should be examined separately to estimate the ROM required by each.

3.4 EVALUATING SYSTEM PERFORMANCE

As discussed in the previous section, the peripheral interface structure for a system is fairly easy to configure if one assumes that R6520-type devices are used. However, before going too far into hardware construction, it is important that the total system performance be evaluated to minimize the probability that major problems will arise in the later stages of the design.

Evaluating system performance involves first determining whether or not the processor is capable of processing all interrupts with the speed required,

and then determining that the processor has sufficient time to perform non-interrupt operations.

The prioritized interrupt structure assumes that, at times, more than one interrupt will occur and that there will be delays encountered in servicing some interrupts caused by the presence of other interrupts. This structure will perform satisfactorily if these delays are not too great.

The interrupt processing time should be evaluated starting with the highest-priority interrupt, then going to the next-highest priority, each time keeping in mind the total time which can be lost due to concurrent higher-priority interrupts. Each time an interrupt is examined, the worst microprocessor response time which can be encountered should be estimated. If this time is still adequate for the function being handled by the interrupt, then that aspect of the system operation can be expected to perform satisfactorily.

The ability of the R650X microprocessors to handle interrupts quickly and conveniently represents one of the real strengths of this microprocessor family. However, in any system being developed, it is important that the percentage of processor time spent servicing interrupts not be so large that the internal data handling, arithmetic operations, etc. cannot be executed properly.

Since the interrupts are usually asynchronous and are not related directly to the main line program, the time lost to interrupts can usually be viewed as an average percentage of the total time. The speed with which the main program can be executed will be reduced by this percentage.

The interrupt service routines are usually short and easy to evaluate. However, the main program is much more difficult to estimate. Fortunately, it is also usually much less critical. Those operations which must meet a particular speed requirement can be examined in detail by the programmer to determine the execution time. This estimated execution time must then be reduced to allow for the time lost to interrupts.

The final step in ensuring satisfactory system performance is a worst-case analysis. This is to determine if there are any places in the program where worst-case interrupts can cause excessive delays in the execution of other programs being executed. Although the effort involved in a complete worst-case analysis is usually excessive, this is one part of the system development task which can lead to significantly greater assurance of success for the entire development process.

SECTION 4

BRINGING UP THE R6500 MICROCOMPUTER SYSTEM

4.1 MICROCOMPUTER TESTING

After many hours of planning, hardware construction, and programming effort, the microcomputer system designer must face what can be his most difficult task: "bringing up" his system. The modern microcomputer with its minimum chip count, and its minimum number of control and data lines, represents a tremendous advance in system design when everything is working properly. However, it can also represent a testing nightmare to the designer who is attempting to troubleshoot the hardware and software which constitute the total design.

A microcomputer lacks many of the things which make testing of conventional logic relatively convenient. To begin with, one simply cannot see most of the control signals, data transfers, etc. which allow the system to operate. In addition, it is impossible to examine directly the contents of the registers and latches which store data within the processor. The data can be examined only indirectly, by looking at the signals on the inputs and outputs to the chip at the proper time.

This problem is compounded by the fact that many programs must be tested "dynamically" -- i.e., the system must be running at its full operating speed with non-recurring events or with a total lack of usable oscilloscope-triggering signals.

For these and many other reasons, it is important that the system designer build effective testing capability into both his hardware and his software. This is particularly true for the pre-production prototypes. When combined with the procedures discussed below, this will minimize both the time and the effort spent in producing that first operational system. After the program and the hardware are completely debugged, many of the testing tools discussed below can be removed from the prototype design without affecting system performance. This allows the designer to arrive at his final production design very shortly after he has proven that the prototypes are operating satisfactorily.

4.1.1 Static Testing

Static testing (i.e., execution of the program), one cycle or one instruction at a time, is the first step in the checkout of any system. In this way, the general flow of the program can be examined and for much of the program the validity of data transfers into and out of memory can be verified. As shown in Figure 4-1, the logic necessary to control RDY to allow Single-Cycle and Single-Instruction Execution is relatively simple. This hardware and its use in system testing are discussed below.

SINGLE-CYCLE EXECUTION

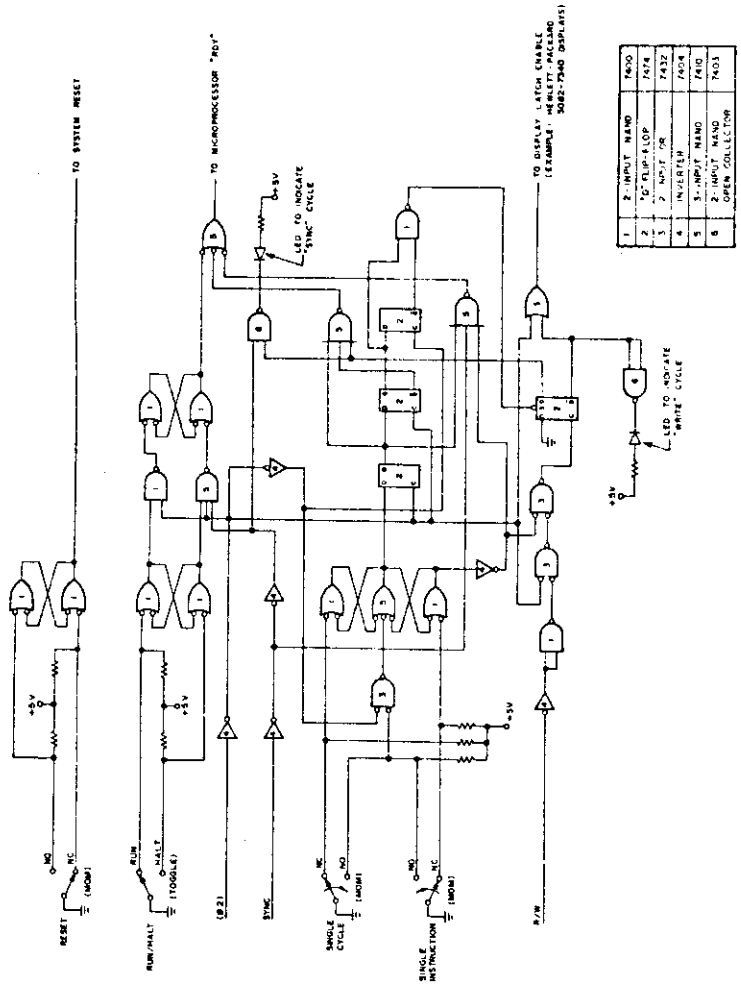
The timing required for Single-Cycle-Execution is shown in Figure 4-2. In this operation, the RDY line has been brought low (GND) to halt the processor. To allow execution of a single cycle, the RDY line goes high (+2.4V) for one cycle each time the Single Cycle switch is activated. Note that the RDY line goes high while the Phase 1 clock is high and the internal timing counter advances on the next Phase 1 clock pulse.

Single-cycle operation allows stopping the processor in any cycle except a WRITE cycle. This allows detailed examination of all cycles of the instruction fetch operation. In addition, it permits detailed examination of operand fetches. Thus, it is possible to verify the operation of most of the hardware involved in memory addressing and control. It is also possible to verify the operation of most of the peripheral interface hardware. This can greatly reduce the time required to test the full dynamic operation of the peripheral device.

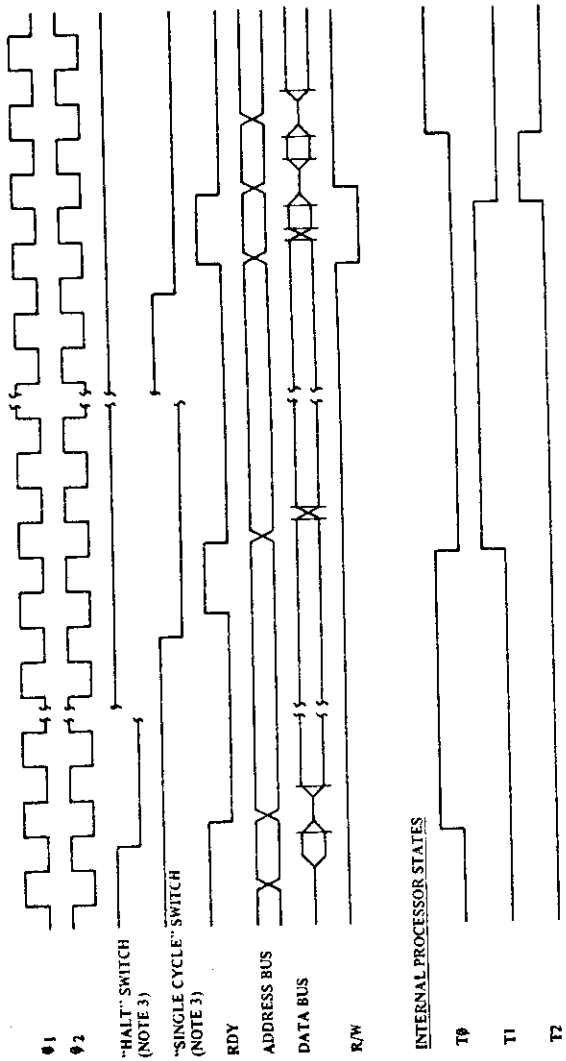
Note that if depressing the Single Cycle switch allows the processor to advance into a WRITE cycle, the processor will complete this cycle and will then stop in the first READ cycle (R/W = 1) which follows. This timing is shown in Figure 4-2.

Appendix A contains a detailed summary of the data which should appear on the address and data lines during each cycle of the R6502 instructions.

Note that the processor often puts out an address and fetches data which it ignores. This is an inherent feature of the processor which uses a "look-ahead" approach to pipelining. Examination of the SYNC signal will allow the designer to keep track of exactly when the data fetched from memory is utilized within the processor and when it is ignored.



Suggested Static Test Control Logic
FIGURE 4-1



NOTES:
1. ⊲⊳ INDICATES AN UNDETERMINED TIME PERIOD DURING WHICH THE SIGNAL WILL CHANGE.
2. THE DATA BUS ENTERS THE HIGH IMPEDANCE STATE DURING EACH PHASE ONE PULSE. HOWEVER, WHILE THE PROCESSOR IS STOPPED THE DATA BUS WILL APPEAR TO REMAIN HIGH OR LOW AS SHOWN.
3. SWITCH ACTUATION IS INDICATED BY A LOW SIGNAL.

Single-Cycle Timing
FIGURE 4-2

A very simple "data trap" can be built into prototype systems to allow examination of the address and data generated by the processor during WRITE cycles. This trap may latch the contents of both the address and data busses or it may latch only the address bus. The latter can be sufficient if a separate means of examining data in memory is provided (see Section 4.2). A suggested configuration for the "data trap" is shown in Figure 4-3. This circuit can be used to display the contents of the address and data busses for both READ and WRITE cycles. The WRITE data are latched and held during the next READ cycle. Depressing the Latch Reset switch then opens the inputs to the latches and allows monitoring of the subsequent READ cycles.

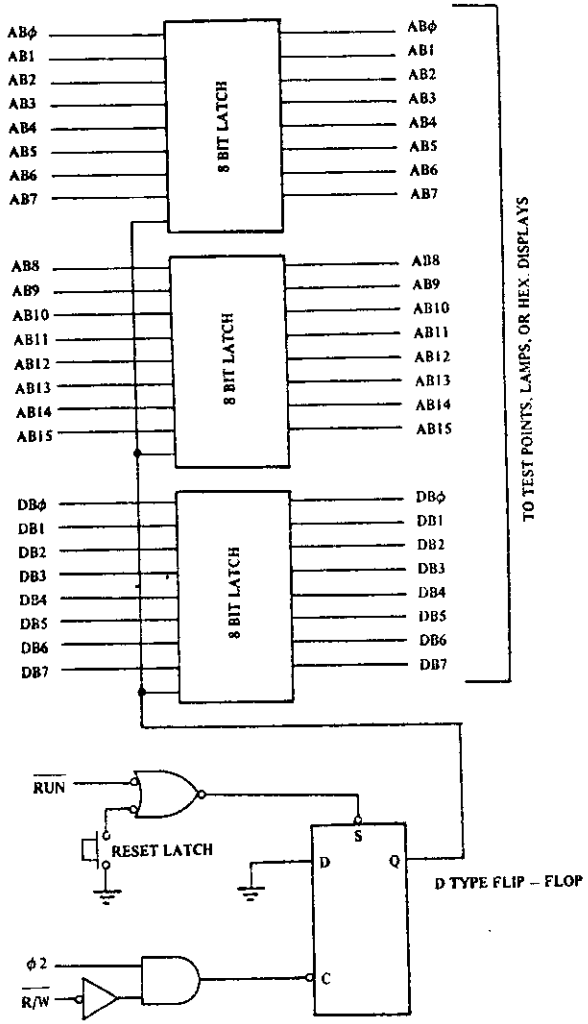
SINGLE INSTRUCTION EXECUTION

While it is extremely useful to be able to analyze the execution of each instruction in detail, it is often sufficient just to look at the general program flow. This is particularly useful when examining the operation of branches and jumps in a program. Single instruction execution is designed to allow this capability on the R6502 which outputs a SYNC signal.

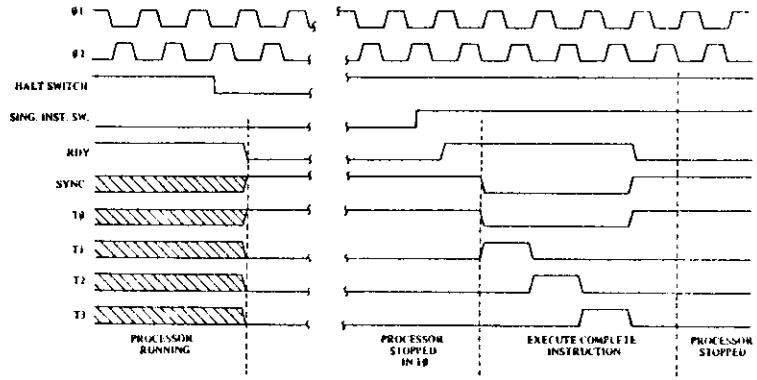
The operation of the single instruction execution logic is based on generation of a SYNC signal within the processor. This signal goes high (> +2.4V DC) during each OP CODE fetch cycle. Single instruction execution is implemented by using SYNC to force RDY low (< +0.4V DC). Under these conditions, the processor will always stop with an OP CODE address on the address bus and the OP CODE on the data bus. The timing for this operation is shown in Figure 4-4. Note that this diagram assumes that the processor is stopped in an OP CODE fetch cycle. Depressing the Single Instruction switch (Figure 4-1) allows execution of that instruction. The processor then stops when the next OP CODE is fetched.

4.1.2 Dynamic Testing

Through static testing techniques, the designer should be able to verify the operation of most of his processor interface hardware, such as the Bus Expanders and Address Decoders (for selecting ROMs, RAMs, etc.). However, this is only a first step to assuring proper system operation. Most peripheral devices cannot be properly tested unless the processor is operating at full speed. This necessitates full dynamic testing.



Microprocessor Single Cycle Data Trap
FIGURE 4-3



Single Instruction Execution
FIGURE 4-4

Dynamic testing generally involves causing the processor to execute a program loop, i.e., to execute a repetitive sequence of instructions. This allows the use of an oscilloscope in examining the processor operation. This repetitive operation can be externally induced through the $\overline{RES}$ or Interrupt ($\overline{IRQ}$ or $\overline{NMI}$) lines, or it can be a part of the program being executed. Both techniques play an important role in the system checkout process.

EXTERNALLY INDUCED LOOPS

The most direct means of causing the processor to execute a loop is to drive one of the direct inputs ($\overline{RES}$, $\overline{IRQ}$ or $\overline{NMI}$) with a signal generator. This technique can be employed to troubleshoot systems which are only partially operational, since it does not rely on proper execution of a particular set of instructions to cause looping to occur. However, this technique can be used only if an oscilloscope can be employed in examining system operation; to do so requires an effective scope-synchronizing signal. For this reason, the following section will discuss not only the signals to be tested and the waveforms which one should see, but also the techniques one may use to assure generation of an effective scope sync.

Probably the most basic operation performed within the processor is the RESET function. Without the RESET hardware and software operating properly, the system will never enter its normal operating mode. For this reason, the first major function to be tested, both statically and dynamically, is the $\overline{RES}$ input.

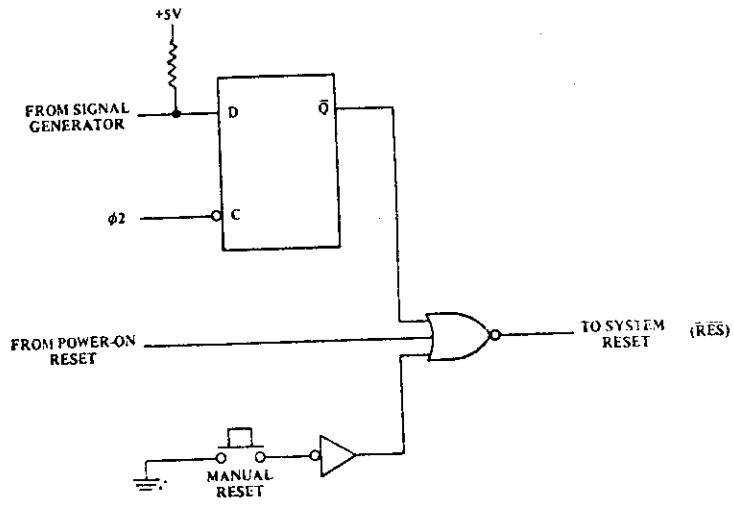
A suggested configuration for dynamically testing the RESET input is shown in Figure 4-5. In this diagram, the RESET input is being driven from a signal generator. Between the signal generator and the processor is a D-type flip-flop to synchronize the chip reset signal to the processor clocks. This synchronizing is extremely important because it stabilizes the data being displayed on the oscilloscope with respect to the scope sync.

The most effective procedure for testing the dynamic operation of the RESET function is to reset the system initially at a rate of approximately one-fifth of the clock rate. This will allow the processor to execute the first few instructions in the reset sequence before being recycled. The designer can then closely examine the timing of address, data and R/W signals. Use of the delayed sweep feature available on most modern oscilloscopes will allow examination of any part of the RESET operation.

When proper operation of the RESET input has been verified, the same technique can be applied to both the $\overline{IRQ}$ and the $\overline{NMI}$ inputs. Driving either of these inputs with a signal generator synchronized to the processor clocks will permit a close examination of the dynamic operation of the interrupt polling sequence. This provides a very important look at the Peripheral Interface selection logic to ensure that all peripheral devices are responding to the proper address.

SOFTWARE LOOPS

During system checkout, the designer must verify the operation of many simple functions which must all operate properly before the entire system is operational. The use of simple software loops will allow a detailed examination of one function at a time. Most importantly, it allows the designer to use an oscilloscope to examine events which may occur very infrequently and which are normally very difficult to see.



Suggested Configuration For Dynamic Reset Testing
FIGURE 4-5

The execution of software loop requires the writing of a program which ends in a JMP back to the beginning of the program. Once the processor enters the loop it will continue to execute the same sequence of instructions until the RESET switch is pushed.

To utilize software loops effectively there must be an event which happens only once each time the processor executes the loop. This signal can be used to trigger the oscilloscope. Including a single WRITE operation in the program allows the R/W signal to be used to trigger the scope. Likewise, careful selection of address in the program will allow use of an address line as a scope sync. Finally, lacking anything else, setting and resetting a peripheral interface device output pin at the beginning of the program provides a very effective sync signal.

4.2 SYSTEM DIAGNOSIS USING HARDWARE PROGRAMMER AIDS

In addition to the techniques described in which the user applies oscilloscopes and his own innovative techniques for analyzing data, Rockwell makes available to the user several hardware aids which assist in the debugging of a microcomputer system and also a software aid called the "Emulator." The hardware aids are a Keyboard Input Monitor (KIM) and a Teletype Input Monitor (TIM). Each of these aids attempts to reduce the problem of debugging the code to the same techniques that are available on a large computer system, and each is designed to allow the debugging of microprocessor code without need to resort to scopes or other data-trapping techniques.

The basic assumption of each of both the KIM and TIM hardware and the Emulator software, is that the microprocessor system is connected correctly, that all of the electrical characteristics have already been checked and met, and that the only problem to be solved is one of debugging programs and I/O hardware which have been entered into the microcomputer.

Each of the hardware techniques assumes that the user will start his design sequence with all of his programming being done in some form of random-access memory which is loadable from an I/O device, examinable by the I/O device, and changeable by the I/O device. This is the normal first step in developing a microcomputer system, and one that should be used prior to committing any of the hardware to PROMs or alterable memory. The only exception to this is if the user is taking advantage of the software Emulator and if his program is such that the Emulator can give him a significant degree of confidence in his coding. In this case the user of the KIM or TIM devices is primarily that of allowing him to have final debugging access to his various memory locations. Therefore, the common characteristic of all these approaches is that by some technique (in the case of the Emulator by reading an input file, in the case of TIM by reading an input tape from the output Cross-Assembler, and in the case of KIM loading a program into memory by hand) the program has been entered into a program storage. Each of these techniques allows the user to initialize various memory and register locations and to

"start execution" of this program at a memory location. Techniques are implemented which permit the user to stop his program at a particular point and analyze the results of the operations which have just been completed. If the results are correct, the coding between the start point and the stop point is correct. If the coding is incorrect, the user analyzes the data which he displays by means of the I/O device and the hardware or software that interfaces it, and determines by inspection of the data and analysis of his coding the error which could cause the results detected.

If the technique of merely analyzing coding is insufficient, each of these systems has the ability to allow the user to go in and re-execute the code with new data or the original data, stopping only at earlier stop-points until he is able to trap the operation that causes the erroneous data to occur. The Emulator has additional features which permit the user to analyze the operation of instructions as they occur which is very useful in determining which part of the program causes operations to be performed incorrectly.

The normal design cycle should actually include a combination of techniques. The user should write his code on a Cross-Assembler and debug much of his loops and non-I/O programming using the Emulator. The Emulator has been designed to allow very easy analysis of data paths, loops and performance of program on a non-hardware basis. It is particularly valuable for the user who is developing routines which have significant loop and subroutining or any completed algorithm.

The use of emulation has the following advantages:

1. It gives the power of a large machine to allow tracing operations which are not feasible at the hardware level.
2. It may indicate prior to the time that the hardware is committed that more memory or more time is required to perform an operation which may dramatically change the hardware implementation to be committed.

In any case, attempting to bring up the microprocessor system without assemblers and an interface module such as TIM is not the most efficient use of the designer's time.

For the user who is just "starting out" with microprocessors, the KIM technique is acceptable because the length and complexibility of the programs to be written should be shorter, and the user can program directly in Hex and debug using KIM exclusively.

4.2.1 KIM -- Keyboard Input Monitor

KIM allows the user to key in Hex values into specified memory locations and to monitor results.

KIM is available to the system designer in several forms. In its simplest form, a single device of the R6530 type including 1024 bytes of preprogrammed ROM may be included as a component in an existing system. The array includes a monitor program which provides the following features:

1. Data input and output control from serial teletypewriters (ASR 33, Silent 700, etc.)
2. Data input and system control from a 22-key keyboard
3. Address and data display on a 6-digit, 7-segment type display

A microprocessor system designed to include the KIM array will allow the designer to perform the following operations:

1. The user may select keyboard (KB) or teletypewriter (TTY) mode for entry, display and control.
2. If in KB mode, the user may enter address or data fields from the keyboard. The user may display the contents of any address location in the system and can modify the contents of any address location (other than preprogrammed ROM locations). The step operation (STEP key) provides a convenient method for displaying the data contained in successive memory locations. Program execution may be authorized to begin from any selected starting address using the RUN key.
3. If in the TTY mode, the user may obtain a printing of the data at any memory location. He can modify the data contained in any memory location. Program listing from any start address to any end address may be authorized. Paper tapes may be loaded or generated automatically. Finally, program execution may be initiated from any selected starting address.
4. In either mode, the user terminates program execution by depressing the STOP key to return control of the system to the KIM program. Alternatively, a depression of the RST key causes a total reset of the system and a return of the system to KIM program control.

The KIM array is also available to the system designer as a part of a special design-in subsystem provided in the form of a printed-circuit card. Included on this card are the following functional elements:

1. R6502 microprocessor array
2. R6530-002 array (containing the KIM monitor program)
3. 22-key keyboard and mode-select switch
4. 6-digit, 7-segment LED display
5. 1024 x 8 RAM
6. R6530-003 array providing an interval timer, 16 I/O pins, and 64 bytes of RAM
7. All interface circuits for operation with serial teletypewriters

This subsystem provides the same operating features described earlier, but is supplied as an operating unit requiring the user to provide only the +5-volt power supply in order to commence operating. As a "stand-alone" subsystem, the KIM permits the user to enter and debug programs of up to 1024 steps and to control the action of up to 16 I/O pins.

For further details on physical and operating characteristics of the KIM array and subsystem, the reader is referred to the KIM manual supplied separately.

4.2.2 TIM -- Teletype Input Monitor

TIM is a pre-programmed R6530. Its application is to allow the user to interface to an ASCII device such as a Teletype, CRT, Execuport, etc. using the ASCII serial communication techniques to communicate to and from the the microprocessor. This effectively allows the user to load memory from the keyboard or from paper tape or cassetts which are attached to his device. By the addition of a single TTL package to the system, TIM can be configured so that it is the starting point for the microprocessor, but once the initialization has been accomplished it transfers itself out of the start-up memory, changes the rest of the microprocessor memory to normal configuration, and operates transparent to the microprocessor.

The proper time for using TIM to develop a microprocessor system is primarily after the system is determined to be wired correctly by the techniques already described. TIM is then utilized to debug the user's code by allowing the user to input prespecified values, execute portions of the code, and examine the results.

It should be noted that because I/O devices are extensions of memory debugging techniques are simplified. They can be configured to control I/O devices to test that lights can be lit, switches tested, motors started and stopped, etc. For instance, all of the connections to lights and switches can be checked from the teletype keyboard by writing into the I/O registers the appropriate code for turning on the lights. Correct operation of switches can be checked without the program running by putting the switches in either state and reading the I/O device result indicated to the programmer. This type of checking totally "shakes out" the I/O connections to make sure the I/O device is located in the correct memory address determines that the wiring to in the correct memory address, determines that the wiring to the I/O devices is correct, and checks on the microprocessor bus.

A rational technique for applying either TIM or KIM is to interconnect the device into the system to get the microprocessor to pass the single-step start-up sequence, and then to use the debugging capability of the TIM prior to executing any of the user's code to verify that all input/output connections are correct. In cases concerned with the stopping of the motors and other devices which require timing, the proper connection to the motors and other devices can be checked without the motor itself physically being checked by disconnecting leads, opening up connectors, and verifying with a 'scope or a meter that the microprocessor's influence at that point is as would be expected on a static basis. Therefore, this technique is recommended as the second step of a start-up sequence.

Significant details are given in the section on the use of restart or start sequence and a single cycle operation to verify the interconnection of most of the system. It should be recalled that the instructions were given independent of the coding that was available to the programmer.

The advantage of using the TIM or KIM in the start-up checkout is that there is known code which is guaranteed to be accurate that should be evoked during this start-up sequence. By referring to the coding of the ROM as it appears in the documentation on the TIM or KIM, the user can apply the known sequences from the TIM or KIM program to verify the start-up sequence, thereby removing one more variable. Therefore, all initial system check-out should be accomplished using TIM or KIM program first in the start-up

sequence to make sure that the interconnection to TIM and to memory are correct. Then, once the basic operation of TIM has been verified, there is a known sequence which TIM will follow dynamically that allows the user to verify that TIM is operational. The user should then verify the remainder of the memory and I/O connections by writing and reading in the memory locations using the debugging feature of the TIM or KIM. This procedure verifies the connection and operation of each of the chips of the system as well as all the interconnections to all outboard devices.

Now the problem is truly reduced to making sure that the programmer's code is correct and the user's program can be loaded by means of either through-the-keyboard or through-the-auxiliary devices.

The program can be debugged as a program rather, with no concern as to whether or not the problem is one of hardware or software. By definition other than incorrect timing to I/O devices, the problem is reduced to one of programming mistakes.

For a more detailed discussion on the programming on TIM, the user is referred to the TIM manual supplied separately.

4.3 MICROPROCESSOR START-UP PROCEDURE

This section attempts to tie together all of the techniques previously discussed into one ordered procedure. This procedure is based on experience gained in bringing up systems using processors from several different manufacturers. While it is certainly true that no single procedure can be expected to catch all of the software and hardware errors that can exist in microcomputer systems, it is hoped that this step-by-step approach will allow the designer to bring up his system with an absolute minimum of difficulty.

This procedure assumes the existence of Single Cycle and/or Single Instruction logic. Any of the System Development tools discussed in Section 4.2 will assist the user in bringing up his system. These devices allow convenient entry of test programs as well as modification of the system program and data.

Each step in the procedure includes the following information:

- Section of the system hardware/software to be checked.
- Hardware, test equipment, etc. required to perform the test.
- Action to be taken in implementing the test.
- Expected results.
- Suggested procedures for analyzing failure modes.

It cannot be emphasized too strongly that one must utilize a very methodical, step-by-step procedure aimed at solving a single problem at a time within the system. It is very easy for several problems to amplify each other to such an extent that nothing within the system seems to be operating properly. Correcting problems one-at-a-time will ultimately yield a complete working system with minimum frustration.

4.3.1 System Power

It is generally recommended that first prototypes of microcomputer systems be built using sockets for the ICs (processor, memories, etc.). One distinct advantage of this technique is that it permits the designer to verify that V_{CC} and V_{SS} are properly connected to each socket before the chips are inserted. The V_{CC} line should be within the tolerances specified about the 5 volt nominal relative to V_{SS}. This basic first step can help avoid power supply connections which may be fatal to the chips in the system.

After checking power connections with a voltmeter or oscilloscope, to insert the processor into its socket and verify that the additional current drain is within specifications for this device.

Before inserting the other devices, examine the address lines, SYNC line and the output clocks to make sure that the processor is generating signals. The address lines should be incrementing and the sync line should be generating regular, positive going pulses. The $\overline{RES}$ line and the RDY line should be high (> +2.4V) for this test.

If the processor appears to be operating and power consumption is reasonable, the rest of the devices in the system can be inserted into their sockets.

4.3.2 Basic System Timing

Before one can expect a microprocessor system to function, proper operation of the basic system timing signals ($\emptyset_1$, $\emptyset_2$, etc.) must be verified. The most important of these signals is the system clock.

In the 6502, both phases ($\emptyset_1$ and $\emptyset_2$) are available for driving the rest of the system. In this system it is necessary to check the clock timing very carefully to assure that the timing of the clock signals within the processor is compatible with that used on the support chips.

Using an oscilloscope, compare the $\emptyset_1$ input clock and the $\emptyset_2$ clock presented to the support chips to verify that the delay due to clock buffering does not exceed the allowable maximum.

4.3.3 System Reset

Static and dynamic analysis of the Reset function can provide very detailed information on how the system is operating. In fact, it is this step which will verify the operation of most of the basic system hardware. The tools required are:

- Single-Cycle/Single-Instruction Logic
- Oscilloscope
- Signal Generator (for Driving RESET)

STATIC ANALYSIS OF SYSTEM DETAILS

Depress the HALT button and then the manual RESET switch: then push the single-cycle switch six times. This will step the processor through the first part of the BRK sequence and into the RESET vector fetch. At this time the processor should be generating FFFC on the address bus and the ROM should have put the low-order byte of the RESET vector onto the data bus in response to this address. This is an excellent time to check the following very basic items:

1. Address Lines

   Using the oscilloscope, verify that the logic levels on the address lines are proper and that they are reflected properly through any bus expanders onto the memory and peripheral chips. This is a very common circuit fault.

2. ROM/PROM Chip Select

   Using the oscilloscope, verify that the address FFFC does select the ROM which contains the low-order byte of the RESET vector.

3. Data Bus

Using the oscilloscope, verify that the voltages on the data bus pins of the processor are proper. It is important for these signals to be analyzed at the processor to ensure proper operation of any bidirectional bus expanders in the system. In this test, the most common indication of improper operation of the data bus expanders is "floating" processor data bus pins, i.e., the processor data bus pins are being driven neither high nor low because the bus expanders are in the open-circuit condition or are reversed.

4. Miscellaneous Processor Pins

Using the oscilloscope, briefly examine the other processor pins (R/W, $\overline{IRQ}$, $\overline{NMI}$, etc.) to assure that there are no voltage level problems detectable at this point. Both of the interrupt inputs and the R/W output should be high. Examine the R/W signal on the input to the memory and peripheral devices.

After these initial tests have been performed, it should be possible to press the single-step switch once more to fetch the high-order byte of the interrupt vector from address FFFD. On the next actuation of the single-cycle switch, the processor address bus should contain the RESET vector which was fetched from memory.

At this point, the processor is ready to execute the system initialization routine. During initialization, it can be expected that program memory will be accessed, peripheral registers will be loaded, and internal processor registers will be cleared or set to a starting value. It is extremely useful to execute this routine one instruction at a time to determine that each time program memory is accessed, the proper instruction is returned. However, unless a data trap is provided, it will be more meaningful to utilize dynamic analysis techniques to analyze the operation of peripheral devices, since most peripheral accesses will be for the purpose of writing either the I/O control or the control registers in the peripheral devices.

DYNAMIC ANALYSIS OF SYSTEM DETAILS

The general technique of dynamic analysis is discussed in Section 4.1.2. The discussion which follows will apply this technique to analyze many of the details of the system operation.

Set up the system as described in Section 4.1.2. After the test equipment is operating properly, most of the system operation can be verified using only the oscilloscope.

ADDRESS BUS VERIFICATION

The first item which must be checked is the specific timing of the address lines. These lines will change during the first part of $\emptyset_1$ but after the specified period, they should stabilize and remain stable through the rest of the cycle. Figure 4-6a shows the waveform which one should expect to see while examining $\emptyset_1$, $\emptyset_2$ and two address lines. In this illustration, one address line is going high and the other is going low. These lines are being generated within the processor and are guaranteed to operate properly provided the total loading on the pins is within specifications. The most common cause of both voltage-level and rise-time problems is overloading. Voltage-level problems are commonly evidenced by the "zero" level being too high, i.e., the address buffer is being asked to sink too much current. Excess capacitance is usually evidenced by the rise and fall times being too long (Figure 4-6b).

In examining the address lines, it is important that the data be examined on the processor and directly on the various support chips. This will assure that any bus expanders in the system are operating properly and that the addresses are valid where they are actually being used.

DATA BUS VERIFICATION

After the addresses have been verified, the next step is to examine the data bus to verify the validity of data being transferred both from the processor to the support chips and from the support chips back into the processor.

Figure 4-7 illustrates the waveform which one can expect to see on the data bus lines. It is very important to note that during $\emptyset_1$ there is no way to predict the voltage on the data bus, since neither the processor nor the support chips are driving these lines. However, during $\emptyset_2$ the data bus pins should go either high or low. It is only during $\emptyset_2$ (high) that the validity of the data can be verified.

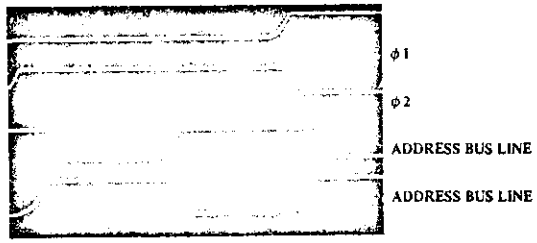
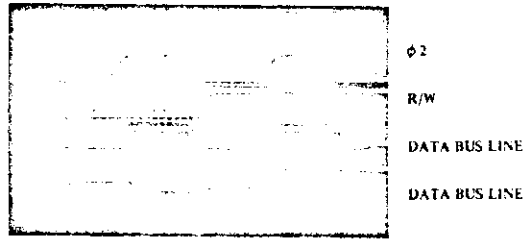


FIGURE 4-6a – Proper Address Lines

FIGURE 4-6b – Excess Address Line Loading

Address Lines In R650X Systems
FIGURE 4-6



The Data Bus in R650X Systems
FIGURE 4-7

Three very important parameters must be considered when examining the data bus. These are the voltage levels, the time at which the data is valid and the delay from the trailing edge of $\emptyset_2$ to data becoming invalid.

1. Voltage Levels

   The logic levels on the processor data bus must always be greater than 2.4 volts for a logic 1 and less than 0.4 volts for a logic 0. This is a very basic concept, but a quick check on these levels very early in the checkout procedure can help the designer avoid hours of attempting to make a system operate with signals which are actually marginal but which on the surface appear to be satisfactory.

   Another very important item to check is whether or not the logic "0" voltage is actually going negative (below GND). It is very important that the logic signals going into all the chip inputs not be allowed to go below -0.3 volt as indicated in the specifications.

2. Data Valid Time

   The time at which data becomes valid indicates the total time which the processor or memory has available to stabilize the gates and latches used to trap the data within the chip. For this reason the data must not take too long to reach either a valid high "1" or a valid low "0." The primary cause of slow signals on the data bus is excessive loading, either resistive or capacitive. Carefully check the devices which are attached to the bus to make sure that the total loading is within specifications.

3. Hold Time

   The last important consideration,"hold time," is defined as the time between the trailing edge of the $\emptyset_2$ pulse and the point at which data is no longer valid. A minimum of 10 ns hold time is required for the processor to trap the data into its internal input latches. The processor internal $\emptyset_2$ pulse is used to gate the contents of the data bus into these latches. Hold time is also required by the various support chips within the system. Carefully check the

signals as they appear on the RAMs, ROMs, etc. to verify that each is being operated in accordance with its specification.

4.3.4 Detailed Component Check

After the dynamic check of the reset routine, the next step is to attempt to run the system program. The success of this operation will determine whether or not a further detailed component check is necessary. It is important to note that the checkout of the system program should proceed one step at a time in much the same manner as we have approached the hardware checkout. If a careful examination has been made of all of the devices, data paths, etc. in the system, the software checkout can proceed under the assumption that the hardware is fully operational. However, it is inevitable that doubts will arise. There are times in the software checkout process that the program will appear to be incorrect ... data will not be going into memory as it should ... or, in general, some hardware failure will be indicated. As soon as this happens, the suspected components should be examined in detail. In keeping with the policy of "one step or one problem at a time," it is important that potential hardware problems not be allowed to invalidate the effort being put into the software checkout.

Component problems can be one of two types: component failure, i.e., a part not operating per specifications; or system failure, i.e., a part being used wrong in the system. The latter problem can be a result of incorrect system design or incorrect wiring. The problem of functional components not operating properly in the system is the one which will be addressed here. In fact, if there is any doubt about a component being functional, it should be replaced immediately upon verification of proper signals to all inputs. If it still does not operate properly, the problem is most likely system-related.

The detailed component check is performed most effectively by loading a small looping program into the system RAM. For this reason, the TIM or KIM debug software (see TIM and KIM Manuals) can be of significant value in this process. The procedure involves static and dynamic operation of a small test program which exercises each of the components in the system. The goal of this step should be a complete verification that all chip selects are operating properly, that all data address lines are operating properly, and that the support chips are driving the processor properly.

The suggested procedures for checkout of each type of component are discussed below.

1. ROMs (PROMs)

The most straightforward component in any microprocessor system is the ROM. This device simply puts out an 8-bit word onto the the data bus in response to an address. Difficulty with ROMs is usually caused by improper chip selects or by misapplication of devices which are not part of the R6500 family. For this reason, static testing of ROMs is usually a very effective first step. This requires entering a test program into RAM and executing this program using the single-cycle switch. The program itself should simply perform a READ (for example, an LDA or LDX instruction) of a selected word for each ROM chip to be tested. The chip selects can then be examined and, at the same time, the address lines presented to the chips can be examined along with the data put on the data bus.

After the chip select, address bus and data bus have been verified statically, it may be necessary to execute the same test program dynamically to assure that all chips in the system are operating at system speed. At this point, it may be necessary to include a WRITE operation (STA, STX, STY, etc.) in the loop to provide a sync signal.

Analysis of the dynamic operation of the ROMs should involve first looking at each address and data bus lines directly on the processor chip. It is here that the address is being generated, and it is here that the data must meet a speed specification. If data are not valid at the proper time, the next step is to determine where excessive delay has been introduced into the data path from address output, through the ROM and back to the processor data bus. It should be kept in mind that it is this entire path which must operate at speed to assure proper processor operation. In fact, if the delays are excessive, it may be necessary to slow down the system clock rate to allow the program data to reach the processor in time. An alternative solution to this problem is the implementation of the RDY signal to hold the processor for one cycle each time it fetches data or program from the ROMs.

Although the problems discussed above may be encountered at this point, it is much more likely that a wiring error will cause a single address or data line to be excessively loaded so that it operates slowly or not at all. This problem can usually be detected and fixed quite easily by looking at each component in the data path.

2. RAMs

Operation of the RAMs in a microprocessor system can be checked in much the same manner as the ROMs. Execution of a test loop program both statically and dynamically for each chip in the system should be sufficient to verify proper operation of the RAMs in the system. For each RAM, both a WRITE and a READ operation should be included in the test loop. This will allow checkout of data transfers in both directions.

During single-cycle execution of the test loop, the processor will stop only in the RAM read operations. However, this will allow a static check of the chip select logic and the address and data lines. Running the program dynamically will allow verification that the data and address signals presented to the RAMs during the WRITE operation are within specification for the RAM being used in the system, and that the total delays through the address, RAM, and data bus path are within specifications for the processor during the READ operations. As with the ROMs, the most likely problem to be encountered at this point is concerned with wiring errors which cause a specific device to operate improperly. A careful check of each pin will enable detection of this type of problem.

3. PIAs

The peripheral interface devices (6520, 6530, etc.) can all be checked out in the manner described above. However, since these chips do many different operations, the test program must be much more complex than that required for the ROM and RAM.

However, it can usually be limited to testing only those functions which are used in the system.

A large part of the operation of the peripheral interface devices can be verified by performing a WRITE followed by a READ for each register on the chip. This will permit a complete checkout to be made of the data paths between the processor and the chips, as well as of all the chip select functions. However, a more complete analysis may be required to verify that data are appearing properly on the output pins of the peripheral chip, and that data on the inputs are being reflected properly back into the processor. This will involve disconnecting the peripheral subsystem which the processor is attempting to drive, and manually putting data into the inputs. A separate test can verify the validity of output data.

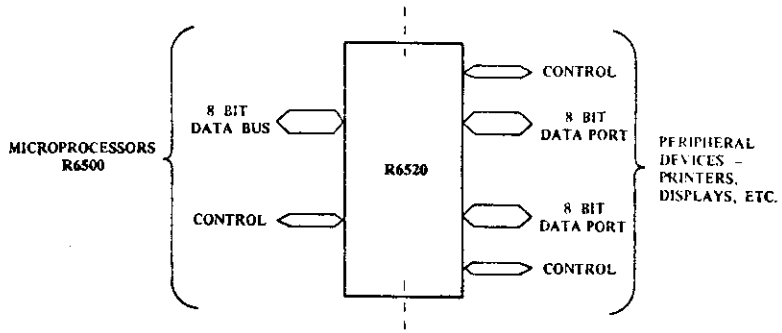
After the system hardware has been examined to the detailed degree discussed above, the designer will have developed confidence that his system can operate properly once the system program is completely debugged. Verification of the system program should proceed with a section-by-section checkout as discussed above. Each subroutine, interrupt routine, etc. should be examined separately. Subroutines, routines, etc. can then be combined to form the major peripheral operating routines, arithmetic routines, etc. which make up the system program. The final result should be a functioning program that has been examined in all of its details, running on a system which is fully operational.

SECTION 5

R6520 PERIPHERAL INTERFACE ADAPTER (PIA)

The R6520 is a direct pin-for-pin replacement for the Motorola M6820 Peripheral Interface Adapter, the "PIA." As such, it meets all of the "PIA" electrical specifications and is totally hardware-compatible with the M6820.

The R6520 is an I/O device which acts as an interface between the microprocessor and peripherals such as printers, displays, keyboards, etc. The prime function of the R6520 is to respond to stimuli from each of the two worlds it is serving. On the one side, the R6520 is interfacing with peripherals via two 8-bit bidirectional peripheral data ports. On the other side, the device interfaces with the microprocessor through an 8-bit data bus (this is the same data bus discussed at length in Section 1.2.2). It is, therefore, simplest to view the basic function of the R6520 as illustrated in the block diagram of Figure 5-1.



Basic R6520 Interface Diagram
FIGURE 5-1

In addition to the lines described above, the R6520 provides four interrupt input/peripheral control lines and the logic necessary for simple, effective control of peripheral interrupts. No external logic is required for interfacing the R650X microprocessor to most peripheral devices. Figure 5-2 shows the R6520 pinout designations for the Peripheral Interface Adaptor.

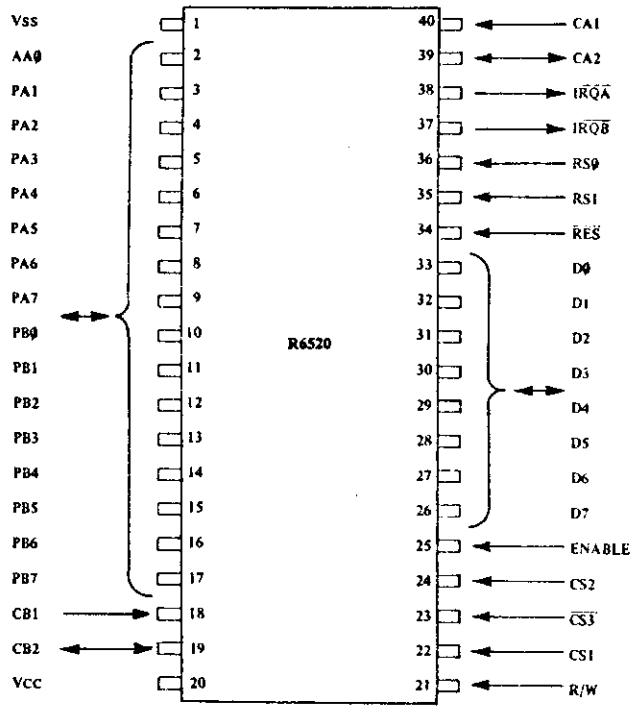
The functional configuration of the R6520 is programmed by the microprocessor during systems initialization. Each of the peripheral data lines is programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of four possible control modes. This allows a high degree of flexibility in the overall operation of the interface.

Some of the more important features of the R6520 are the following:

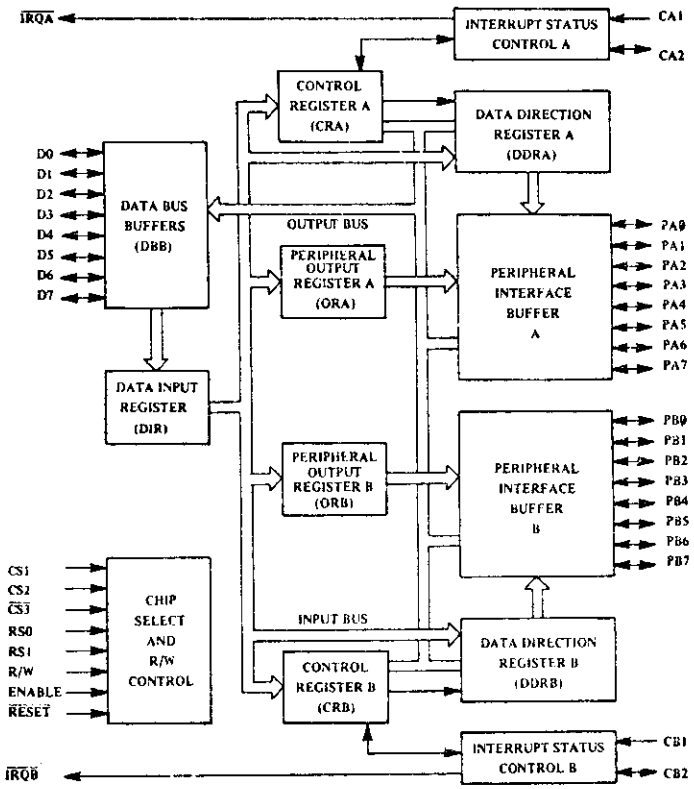
- Compatibility with the R6500 microprocessors (CPUs).
- Eight-bit bidirectional data bus for communication with the microprocessor.
- Two 8-bit bidirectional ports for interface to peripherals.
- Two programmable control registers.
- Two programmable Data Direction Registers.
- Four individually controlled interrupt input lines -- two usable as peripheral control outputs.
- Handshake control logic for input and output peripheral operation.
- High-impedance three-state and direct transistor drive peripheral lines.
- Program-controlled interrupt and interrupt mask capability.

5.1 R6520 ORGANIZATION

Figure 5-3 contains a block diagram of the R6520 showing the internal registers and data paths and the various inputs and outputs on the device. This section contains a general description of the internal organization of the device, along with a discussion of how the various registers affect one another. The following sections discuss the details



R6520 Pinout Designations, Peripheral Interface Adaptor
FIGURE 5-2



R6520 Internal Architecture

FIGURE 5-3

of the inputs and outputs on the chip, along with a detailed discussion of the operation of each register. The final section discusses the R6520 from an operational viewpoint, describing the interaction of the register bits, input/output lines, etc.

The R6520 is organized into two independent sections referred to as the "A Side" and the "B Side." Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control and the buffer necessary to drive the Peripheral Interface busses.

5.1.1 Data Input Register

When the microprocessor writes data into the R6520, the data which appear on the data bus during the Phase 2 clock pulse is latched into the Data Input Register. It is then transferred into one of six internal registers of the R6520 after the trailing edge of Phase 2. This assures that the data on the peripheral output lines will not "glitch" -- i.e., the output lines will make smooth transitions from high to low or from low to high, and the voltage will remain stable except when it is going to the opposite polarity.

5.1.2 Control Registers (CRA and CRB)

The Control Registers allow the microprocessor to control the operation of the interrupt lines (CA1, CA2, CB1, CB2), and peripheral control lines (CA2, CB2). A single bit in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB) discussed below. In addition, two bits (bit 6 and 7) are provided in each control register to indicate the status of the interrupt input lines (CA1, CA2, CB1, CB2). These interrupt status bits ($\overline{IRQA}$, $\overline{IRQB}$) are normally interrogated by the microprocessor during the interrupt service program to determine the source of an active interrupt. These are the interrupt lines which drive the interrupt input ($\overline{IRQ}$, $\overline{NMI}$) of the microprocessor. The other bits in CRA and CRB are described in the discussion of the interface to the peripheral device (Section 1.5.4).

The various bits in the control registers will be accessed many times during a program to allow the processor to enable or disable interrupts, change operating modes, etc. as required by the peripheral device being controlled.

5.1.3 Data Direction Registers (DDRA, DDRB)

The Data Direction Registers allow the processor to program each line in the 8-bit Peripheral I/O port to act as either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port, and each bit in DDRB controls the corresponding line in the Peripheral B port. Placing a "0" in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input, while a "1" causes it to act as an output.

The Data Direction Registers are normally programmed only during the system initialization routine which is performed in response to a Reset signal; however, the contents of these registers can be altered during system operation. This allows very convenient control of some peripheral devices such as keyboards.

5.1.4 Peripheral Output Registers (ORA, ORB)

The Peripheral Output Registers store the output data which appear on the Peripheral I/O port. Writing an "0" into a bit in ORA causes the corresponding line on the Peripheral A port to go low (< 0.4V) if that line is programmed to act as an output. A "1" causes the corresponding output to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

Addressing of these registers is discussed in Section 5.2.4.

5.1.5 Interrupt Status Control

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control (A, B). This logic interprets the contents of the corresponding Control Register, detects active transitions on the interrupt inputs and performs those operations necessary to assure proper operation of these four peripheral interface lines. The operation of these lines is described in detail in Section 5.3.2

5.1.6 Peripheral Interface Buffers (A, B) and Data Bus Buffers (DBB)

The Buffers which drive the peripheral I/O ports and the data bus provide the current and voltage drive necessary to ensure proper system operation and to meet the device specifications.

5.2 PROCESSOR INTERFACE

The R6520 interfaces to the microprocessor with an 8-bit bidirectional data bus, 3 chip-select lines, 2 register-select lines, 2 interrupt request lines, read/write line, enable line, and reset line.

5.2.1 Data Bus (D0-D7)

The 8-bit, bidirectional data bus allows the transfer of data between the microprocessor and the R6520. The data bus output drivers are 3-state devices that remain in the high impedance state except when the microprocessor reads data from the peripheral adapter. This data bus is the same as discussed in Section 1.2.2, "Bus Structure."

5.2.2 Enable (E)

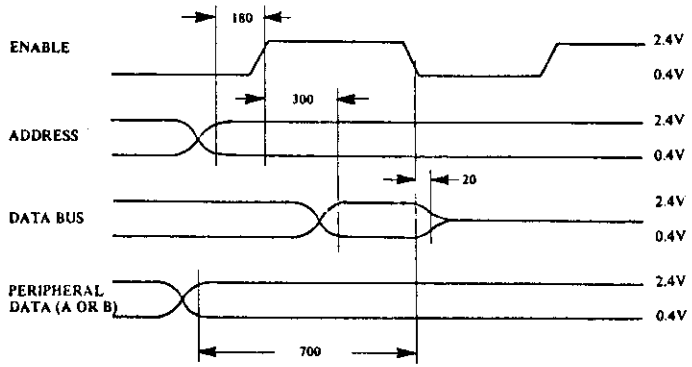
The Enable input is the only microprocessor interface timing input on the peripheral interface device. All data transfers into and out of the R6520 are controlled by this signal. In normal operation, this input should be connected to the phase two clock signal. In the case of the R6512 through R6515, this is the Phase 2 clock generated externally to the microprocessor chip. For on-chip oscillator products the enable pulse becomes Ø2(OUT).

5.2.3 Read/Write (R/W)

This signal is generated by the microprocessor to control the direction of data transfers on the data bus. A "low" (< 0.4V) on this line enables the input buffers (microprocessor Write), and data are transferred from the microprocessor to the R6520 under control of Enable input if the device has been chip-selected. A "high" on the R/W line allows the R6520 to transfer data to the data bus buffers. The data bus buffers are enabled when the proper chip-select and Enable signals are present. Figure 1.23 illustrates the Read/Write timing.

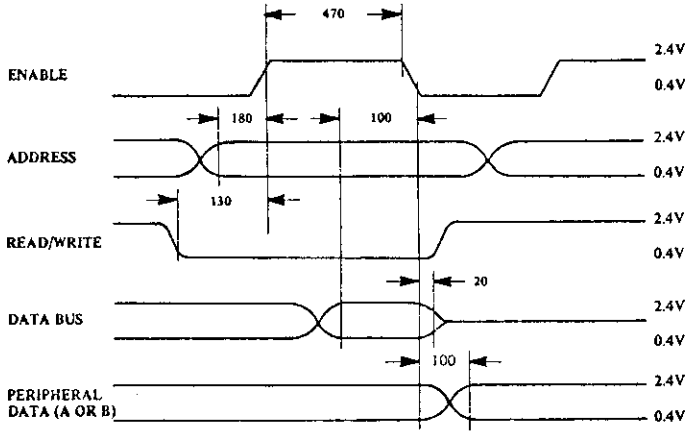
5.2.4 Chip Select Lines (CS0, CS1, CS2)

These three inputs allow the microprocessor to select the proper peripheral interface device. CS0 and CS1 must be high and CS2 must be low for selection of the device. Data transfers are then performed under control of the Enable and R/W signals. These lines are normally connected to the address lines on the microprocessor, either directly or through address decoders.



Microprocessor Interface Timing - Read

FIGURE 5-4 a



*NOTE: ALL TIMES SPECIFIED ARE IN nSEC FOR 1MHZ OPERATION.

Microprocessor Interface Timing - Write

FIGURE 5-4 b

Microprocessor Interface Timing

FIGURE 5-4

As described in Section 5.4.2, a single bit in each Control Register (CRA and CRB) controls access to the Data Direction Register or the Peripheral interface. If bit 2 in the Control Register is a "1," a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0," the Data Direction Register is selected. Internal registers are selected by the Register Select lines (RSØ, RS1) and the Data Direction Register Access Control bit as follows:

RS1	RSØ	Data Direction Register Access Control Bit CRA-2	CRB-2	Register Selected
Ø	Ø	1	-	Peripheral Interface A (See Section 5.2.5)
Ø	Ø	Ø	-	Data Direction Register A
Ø	1	-	-	Control Register A
1	Ø	-	1	Peripheral Interface B (See Section 5.2.5)
1	Ø	-	Ø	Data Direction Register B
1	1	-	-	Control Register B

If the programmer wishes to write the data into DDRA, ORA, DDRB, or ORB, he must first set bit 2 in the proper Control Register. The desired register can then be accessed with the address determined by the address interconnect technique used.

5.2.5 Register Select Lines (RS0), (RS1)

These two register select lines are used to select the various registers inside the R6520. These input lines are used in conjunction with internal control registers to select a particular register that is to be accessed by the microprocessor. These lines are normally connected to microprocessor address output lines. These lines operate in conjunction with the chip-select inputs to allow the microprocessor to address a single 8-bit register within the microprocessor address space. This register may be an internal register (CRA, ORA, etc.) or it may be a Peripheral I/O port.

The processor can write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor can directly read the

contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers, and the two procedures are discussed separately below.

READING THE PERIPHERAL A I/O PORT

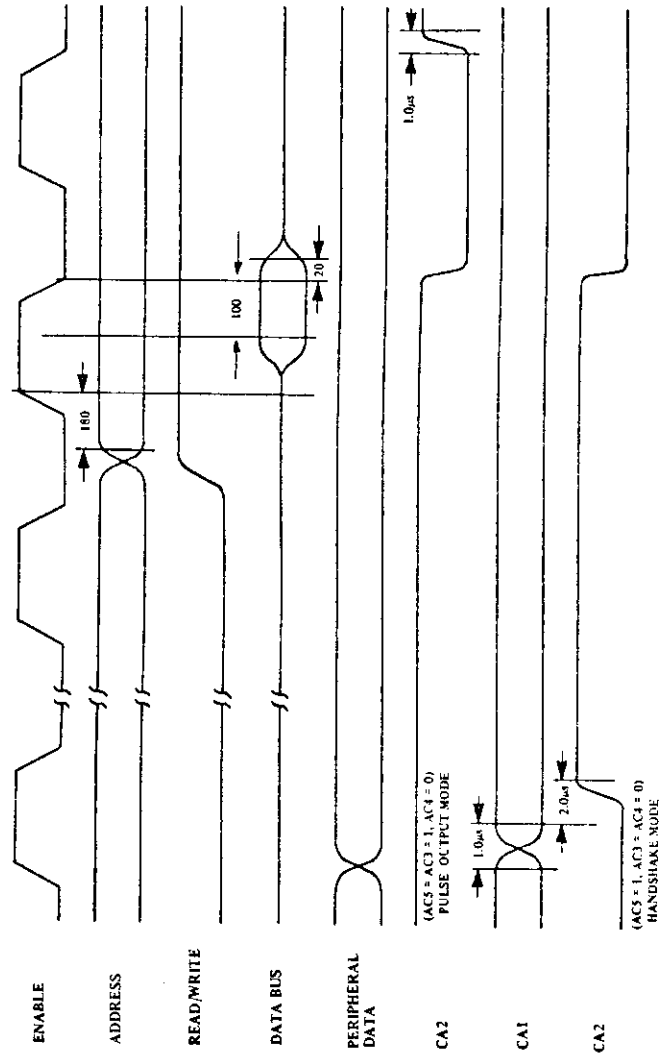
The Peripheral A I/O port consists of 8 lines which can be programmed to act as inputs or outputs. When programmed to act as outputs, each line reflects the contents of the corresponding bit in the Peripheral Output Register. When programmed to act as an input, these lines will go high or low depending on the input data. The Peripheral Output Register (ORA) has no effect on those lines programmed to act as inputs. The eight lines of the Peripheral A I/O port therefore contain either input or output data depending on whether the line is programmed to act as an input or an output. Figure 5-5 illustrates the interface timing.

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines into the processor (via the data bus). This will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read into the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a zero from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

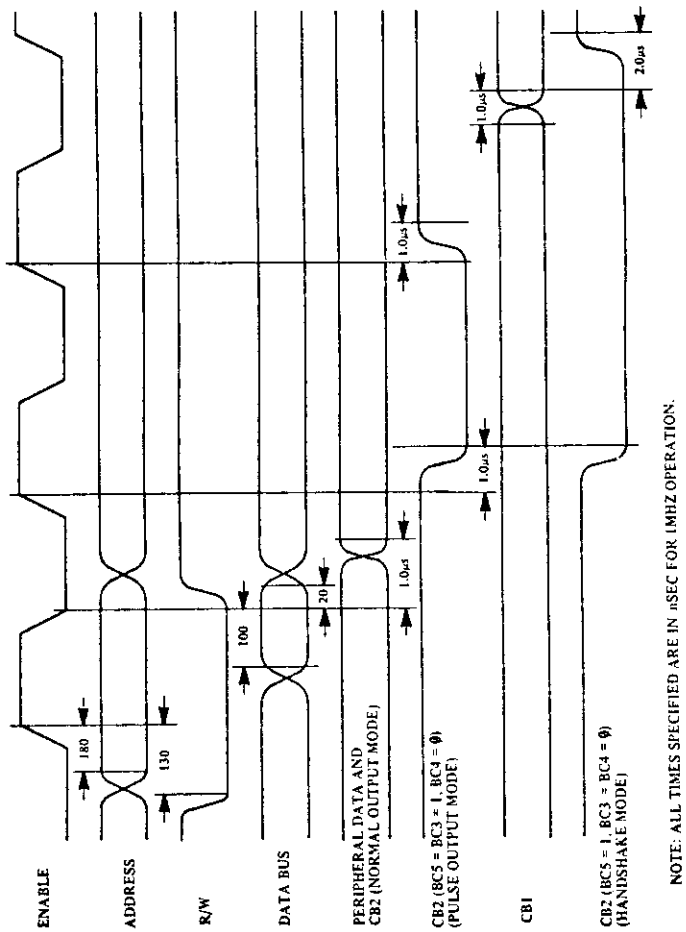
READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data are read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is, therefore, possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back into the processor on a Read operation. Figure 5-6 illustrates the timing.



NOTE: ALL TIMES SPECIFIED ARE IN nSEC FOR 1 MHZ OPERATION.

Peripheral A Interface Timing
FIGURE 5-5



NOTE: ALL TIMES SPECIFIED ARE IN nSEC FOR 1MHZ OPERATION.

Peripheral B Interface Timing
FIGURE 5-6

The details of the Peripheral A and Peripheral B ports will be discussed in the next section under the discussion of the interface between the R6520 and the Peripheral Devices.

5.2.6 Reset ($\overline{RES}$)

The active low Reset line resets the contents of all R6520 registers to a logic zero. This line can be used as a power-on reset or as a master reset during system operation.

5.2.7 Interrupt Request Line ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are "open source" (no load device on the chip) and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a "wired-OR" configuration. The "A" and "B" in the titles of these lines correspond to the "A" peripheral port and the "B" peripheral port. Hence each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers. These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2).

The four interrupt flags are set by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2). Controlling this active transition is discussed in the next section under the discussion of the interface between the R6520 and the peripheral device.

CONTROL OF $\overline{IRQA}$

Control Register A bit 7 is always set by an active transition of the CA1 interrupt input signal. Interrupting from this flag can be disabled by setting bit 0 in the Control Register A (CRA) to a logic 0. Similarly, Control Register A bit 6 can be set by an active transition of the CA2 interrupt input signal. Interrupting from this flag can be disabled by setting bit 3 in the Control Register to a logic 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the proper chip-select and register-select signals are provided to allow the processor to read the Peripheral A I/O port.

CONTROL OF $\overline{IRQB}$

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB is set by an active transition on CB1; interrupting from this flag is controlled by CRB bit 0. Likewise, bit 6 in CRB is set by an active transition on CB2; interrupting from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 are reset by a "Read Peripheral B Output Register" operation.

SUMMARY:

IRQA goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1.

IRQB goes low when CRB-7 = 1 and CRB-0 = 1 or when CRB-6 = 1 and CRB-3 = 1.

The use of these interrupt flags and interrupt disable bits is discussed in more detail in Section 5.3.

It should be stressed at this point that the flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

5.3 PERIPHERAL INTERFACE

The R6520 provides two 8-bit bidirectional ports and four interrupt/control lines for interfacing to peripheral devices. These ports and the associated interrupt/control lines are referred to as the "A" side and the "B" side. Each side has its own unique characteristics and will be discussed separately below.

5.3.1 Peripheral I/O Ports

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by loading data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on

the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

PERIPHERAL A I/O PORT (PAØ-PA7)

As discussed in Section 5.1.3 each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a "1" in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A "0" in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-ups as shown in Figure 5-7a. These pull-up devices are resistive in nature and therefore allow the output voltage to go to Vdd for a logic 1. The switches can sink a full 1.6 ma, making these buffers capable of driving one standard TTL load.

In the input mode, the pull-up devices shown in Figure 5-7a are still connected to the I/O pin and still supply current to this pin. For this reason, these lines represent one standard TTL load in the input mode.

PERIPHERAL B I/O PORT (PBØ-PB7)

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output has been discussed previously. Also, the effect of reading or writing this port has been discussed. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing. These will be discussed below.

The Peripheral B I/O port buffers are push-pull devices as shown in Figure 5-7b. The pull-up devices are switched "OFF" in the "0" state and "ON" for a logic 1. Since these pull-ups are active devices, the logic "1" voltage is not guaranteed to go higher than +2.4V. They are TTL compatible but are not CMOS compatible.

However, the active pull-up devices can sink up to 1 ma at 1.5V. This current drive capability is provided to allow direct connection to Darlington transistor switches. This permits very simple control of relays, lamps, etc.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic which is a function of the Peripheral B push-pull buffers is the high-impedance input state. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high-impedance state. These inputs will then have an impedance of greater than 1 megohm.

5.3.2 Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PAØ-PA7, PBØ-PB7).

PERIPHERAL A INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2)

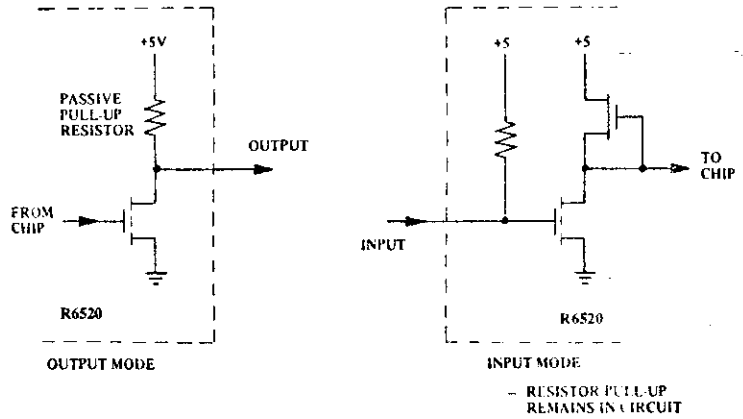
CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of Control Register A to a logic 1. The active transition can be programmed by the microprocessor by setting a "Ø" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition. Note: A negative transition is defined as a transition from a high (> 2.4V) to a low (< 0.4V), and a positive transition is defined as a transition from a low to a high voltage.

Setting the interrupt flag will interrupt the processor through IRQA if bit Ø of CRA is a 1 as described previously.

CA2 can act as a totally independent interrupt input or as a peripheral control output. As an input (CRA, bit 5 = Ø) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

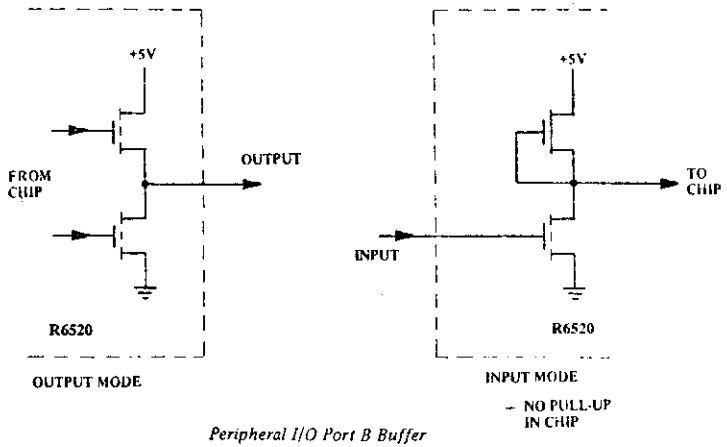
These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupts.

In the Output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a "0" and CRA, bit 3 to a "1." This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.



Peripheral I/O Port A Buffer

FIGURE 5-7a



Peripheral I/O Port B Buffer

FIGURE 5-7b

Peripheral I/O Port Buffers

FIGURE 5-7

A second output mode permits CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available. This technique is discussed in detail in Section 3.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0, respectively.

The operation of CA1 and CA2 is summarized in the next section.

PERIPHERAL B INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CB1, CB2)

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB, bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

The operation of CB1 and CB2 is summarized in the next section. A more detailed discussion of handshaking on the Peripheral B I/O port is contained in Section 3 of this manual.

5.4 R6520 OPERATION

5.4.1 Control Register Operation

	7	6	5 4 3	2	1 Ø
CRA	IRQA1	IRQA2	CA2 Control	DDRA Access	CA1 Control

	7	6	5 4 3	2	1 Ø
CRB	IRQB1	IRQB2	CB2 Control	DDRB Access	CB2 Control

Control Register Bit Designations

FIGURE 5-8

TABLE 5-1

Control of Interrupt Inputs CA1, CB1

CRA (CRB) Bit 1	CRA (CRB) Bit 0	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
0	0	Negative	Disable--remain high
0	1	Negative	Enabled--goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable--remain high
1	1	Positive	Enable--as explained above

*Note 1: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

TABLE 5-2

Control of CA2 (CB2) as Interrupt Inputs (Bit 5 = "0")

CRA (CRB) Bit 5	CRA (CRB) Bit 4	CRA (CRB) Bit 3	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Output
0	0	0	Negative	Disable--remains high
0	0	1	Negative	Enabled--goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable--remains high
0	1	1	Positive	Enable--as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

5.4.2 R6520 Operation in R6500 Systems

A brief review of the overall operation of the R6520 should serve to tie together many of the details discussed previously.

During the system initialization routine which is executed in response to the processor RESET signal, the microprocessor will write a pattern of 1's and 0's into the Data Direction Registers. This will determine those lines which are to act as inputs and those which are to act as outputs.

This pattern will usually be fixed for the system operation. Therefore, the next step would be to set the various operating modes, active transitions, etc. which are controlled by the Control Registers. At the same time, the Data Direction Register Access Control Bit can be set to a 1 to allow the processor to control the Peripheral Ports during system operation.

The interrupts will normally remain disabled until the entire system is initialized. At this time, the interrupts are enabled and full system operation begins.

During system operation, the microprocessor will interrogate the switches, sensors, etc. in the peripheral device by reading the data on the Peripheral Input lines. Binary or decimal data may be transferred into the microprocessor in the same way. At the same time the various lights, motors, solenoids, etc. on the peripheral device are controlled by writing data into the appropriate bits of the Peripheral Output Registers. The entire sequence of operations is determined by the programmer to control a particular peripheral device in a defined manner. The various registers, gates, etc. in the Interface Device act primarily as a link between the internal processor operations and the various inputs and outputs on the peripheral devices being controlled.

TABLE 5-3

Control of CA2 Output Modes

CRA Bit 5	CRA Bit 4	CRA Bit 3	Mode	Description
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

TABLE 5-4

Control of CB2 Output Modes

CRB Bit 5	CRB Bit 4	CRB Bit 3	Mode	Description
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

SECTION 6

R6522 VERSATILE INTERFACE ADAPTER (VIA)

6.1 R6522 ORGANIZATION

The R6522 Versatile Interface Adapter (VIA) provides all of the capability of the R6520. In addition, this device contains a pair of very powerful interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bidirectional data transfers between VIAs in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. Also, several peripheral I/O lines can be controlled directly from the interval timers for generating programmable-frequency square waves and for counting externally generated pulses. To facilitate control of the many powerful features of this chip, the internal registers have been organized into an interrupt flag register, an interrupt enable register, and a pair of function control registers.

Figures 6-1 through 6-3 show the R6522 interfacing, pinout designations, and block diagram, respectively.

6.2 PROCESSOR INTERFACE

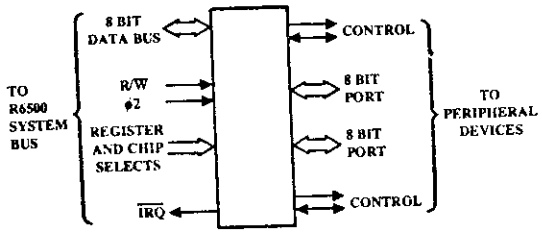
This section contains a description of the buses and control lines which are used to interface the R6522 to the system processor.

6.2.1 Phase Two Clock ($\phi 2$)

Data transfers between the R6522 and the system processor take place only while the Phase Two Clock is high. In addition, $\phi 2$ acts as the time base for the various timers, shift registers, etc. on the chip.

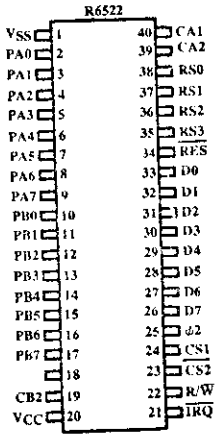
6.2.2 Chip Select Lines (CS1, $\overline{CS2}$)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected R6522 register will be accessed when CS1 is high and $\overline{CS2}$ is low.



R6522 Interface Diagram

FIGURE 6-1



R6522 Pinout Designations

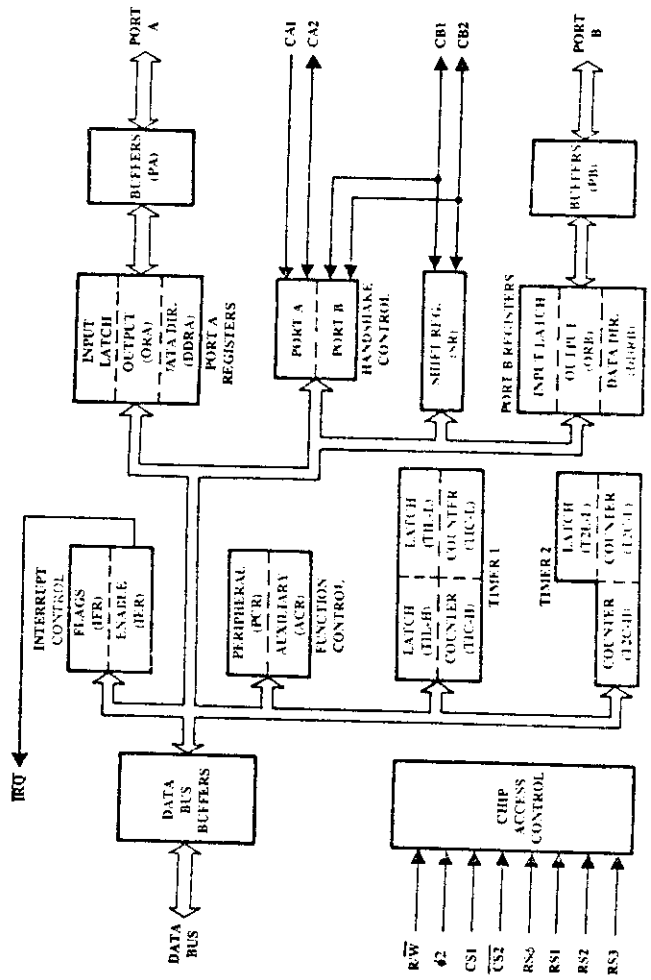
FIGURE 6-2

6.2.3 Register Select Lines (RS0, RS1, RS2, RS3)

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal R6522 register which is to be accessed. The sixteen possible combinations access the registers as follows:

RS3	RS2	RS1	RS0	Register	Remarks
L	L	L	L	ORB	
L	L	L	H	ORA	Controls Handshake
L	L	H	L	DDRB	
L	L	H	H	DDRA	
L	H	L	L	T1L-L	Write Latch
				T1C-L	Read Counter
L	H	L	H	T1C-H	Trigger T1L-L/ T1C-L Transf.
L	H	H	L	T1L-L	
L	H	H	H	T1L-H	
H	L	L	L	T2L-L	Write Latch
				T2C-L	Read Counter
H	L	L	H	T2C-H	Triggers T2L-L/ T2C-L Transfer
H	L	H	L	SR	
H	L	H	H	ACR	
H	H	L	L	PCR	
H	H	L	H	IFR	
H	H	H	L	IER	
H	H	H	H	ORA	No Effect on Handshake

Note: L = 0.4V DC, H = 2.4 V DC.



R6522 Block Diagram

FIGURE 6-3

6.2.4 Read/Write Line (R/$\overline{W}$)

The direction of data transfers between the R6522 and the system processor is controlled by the R/$\overline{W}$ line. If R/$\overline{W}$ is low, data will be transferred out of the processor into the selected R6522 register (write operation). If R/$\overline{W}$ is high and the chip is selected, data will be transferred out of the R6522 (read operation).

6.2.5 Data Bus (DB0 - DB7)

The eight bidirectional data bus lines are used to transfer data between the R6522 and the system processor. The internal drivers will remain in the high-impedance state except when the chip is selected (CS1 = 1, $\overline{CS2}$ = 0), Read/Write is high, and the Phase Two Clock is high. At this time, the contents of the selected register are placed on the data bus. When the chip is selected, with Read/Write low and $\phi 2$ = 1, the data on the data bus will be transferred into the selected R6522 register.

6.2.6 Reset ($\overline{RES}$)

The Reset input clears all internal registers to logic 0 (except T1, T2 and SR). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

6.2.7 Interrupt Request ($\overline{IRQ}$)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-OR'ed" with other equivalent signals in the system.

6.3 PERIPHERAL INTERFACE

This section contains a description of the buses and control lines which are used to drive peripheral devices under control of the internal R6522 registers. The operation of these peripheral interface lines is described in detail in subsequent sections.

6.3.1 Peripheral A Port (PA0 - PA7)

The Peripheral A port consists of eight lines which can be individually programmed to act as an input or an output under control of a Data Direction Register. The level of output pins is controlled by an Output Register and input data can be latched into an internal register under control of the CA1 line.

All of these modes of operation are controlled by the system processor through the internal control registers.

6.3.2 Peripheral A Control Lines (CA1, CA2)

The two peripheral A control lines act as interrupt inputs or as a handshake pair, one input and one output. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A Port input lines. The various modes of operation are controlled by the system processor through the internal Control Registers.

6.3.3 Peripheral B Port (PB 0 - PB7)

The Peripheral B port consists of eight bidirectional lines which are controlled by an output register and a data direction register in the same manner as the PA port. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0 ma at 1.5 VDC in the output mode to allow the outputs to directly drive Darlington transistor switches. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin.

6.3.4 Peripheral B Control Lines (CB1, CB2)

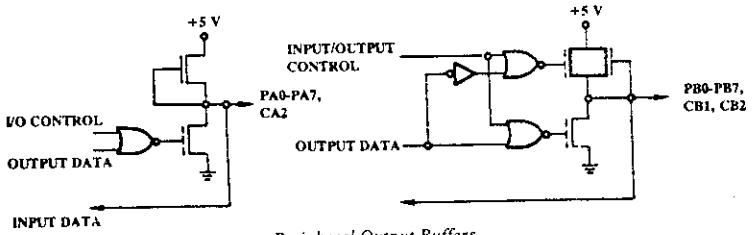
The Peripheral B control lines act as interrupt inputs or as a handshake pair, one input, and one output. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0 ma at 1.5 VDC in the output mode to allow the outputs to directly drive Darlington transistor switches. In addition, these lines act as a serial port under control of the Shift Register.

6.4 R6522 OPERATION

This section contains a discussion of the various blocks of logic shown in Figure 6-3. In addition, the internal operation of the R6522 is described in detail.

6.4.1 Data Bus Buffers (DB), Peripheral A Buffers (PA), Peripheral B Buffers (PB)

The characteristics of the buffers which provide the required voltage and current drive capability were discussed in the previous section.



Peripheral Output Buffers

FIGURE 6-4

6.4.2 Chip Access Control

The Chip Access Control contains the necessary logic to detect the chip select condition and to decode the Register Select inputs to allow accessing the desired internal register. In addition, the R/W and ϕ2 signals are utilized to control the direction and timing of data transfers. When writing into the R6522, data are first latched into a data input register during ϕ2. Data are then transferred into the desired internal register during Phase 2 Chip Select. This allows the peripheral I/O line to change without "glitching." When the processor reads the R6522, data are transferred from the desired internal register directly onto the Data Bus during Phase 2 high.

6.4.3 Port A Registers, Port B Registers

Three registers are used in accessing each of the 8-bit peripheral ports. Each port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A "1" causes the pin to act as an output.

When the pin is programmed to act as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register (ORA, ORB). A "1" in the Output Register causes the pin to go high, and a "0" causes the pin to go low. Data written into Output Register bits corresponding to pins programmed to act as inputs will be unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the data on the PA pins. With input latching enabled (ACR, bit 0), setting the CA1 Interrupt Flag (IFR1) by an active transition on CA1, will cause IRA to latch the contents of the Port A pins until the Interrupt Flag is cleared.

The IRB register operates in a similar manner. However, for output pins, the corresponding IRB bit will reflect the contents of the Output Register bit instead of the actual pin. This allows proper data to be read into the processor if the output pin is not allowed to go to full high voltage, e.g., driving transistors. If input latching is enabled on Port B, setting the CB1 Interrupt Flag will cause IRB to latch this combination of input data and ORB data until the Interrupt Flag is cleared.

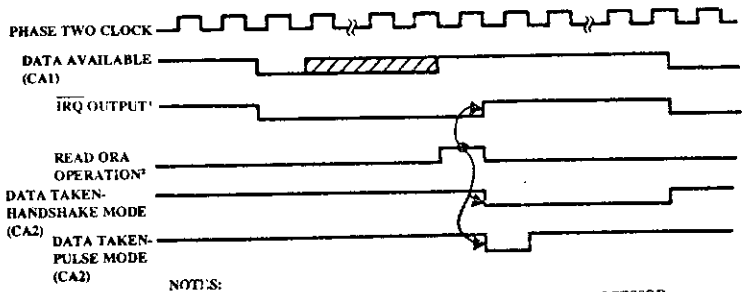
6.4.4 Handshake Control

The R6522 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

READ HANDSHAKE

Positive control of data transfers from peripheral devices into the system processor can be accomplished effectively using "Read" handshaking. In this case, the peripheral device must generate "Data Ready" to signal the processor that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the R6522, automatic "Read" handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The Data Ready signal will set an internal flag which may interrupt the processor or which can be polled under software control. The Data Taken signal can be either a pulse or a DC level which is set low by the system processor and is cleared by the Data Ready signal. These options are shown in Figure 6-5 which illustrates the normal Read Handshaking sequence.



NOTES:

1. SIGNALS "DATA AVAILABLE" TO THE SYSTEM PROCESSOR.
2. $R/\overline{W} = 1$, $\overline{CS2} = 0$, CS1 = 1, RS3 = 0, RS2 = 0, RS1 = 0, RS0 = 1.

Read Handshake Timing Sequence

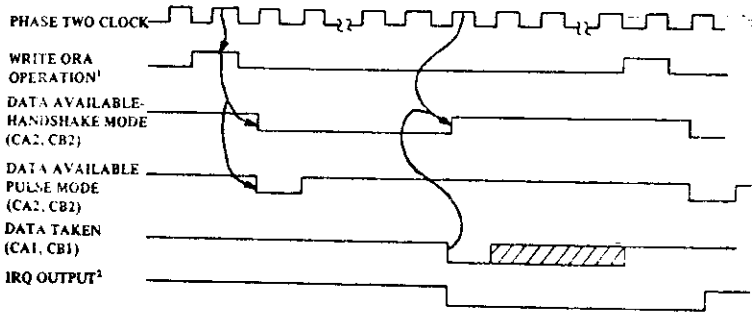
FIGURE 6-5

WRITE HANDSHAKE

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described in Section A for Read Handshaking. However, for "Write" handshaking, the processor must generate the "Data Ready" signal (through the R6522) and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the R6522. CA2 or CB2 acts as a Data Ready output in either the DC level or pulse mode and CA1 or CB1 accepts the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 6-6.

6.4.5 Timer 1

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches are used to store data which are to be loaded into the counter. After loading, the counter decrements at system clock rate, i.e., under control of the clock applied to the Phase Two input pin. Upon reaching zero, an interrupt flag will be set, and $\overline{IRQ}$ will go low if enabled. The timer will then disable any further interrupts, or will automatically transfer the contents of the latches into the counter and will continue to decrement. In



NOTES:

1. $R/\overline{W} = 0$, $\overline{CS2} = 0$, CS1 = 1, RS3 = 0, RS2 = 0, RS1 = 0, RS0 = 1.
2. SIGNALS "DATA TAKEN" TO THE SYSTEM PROCESSOR.

Write Handshake Timing Sequence

FIGURE 6-6

addition, the timer can be instructed to invert the output signal on peripheral pin PB7 each time it "times-out." Each of these modes is discussed separately below.

WRITING THE TIMER 1 REGISTERS

The operations which take place when writing to each of the four Timer 1 addresses are as follows:

RS3	RS2	RS1	RS0	Operation ($R/\overline{W}$ = L)
L	H	L	L	Write into low-order latch.
L	H	L	H	Write into high-order latch Write into high-order counter. Transfer low-order latch into low order counter. Reset T1 interrupt flag. (IFR6)
L	H	H	L	Write low-order latch.
L	H	H	H	Write high-order latch. Reset T1 interrupt flag. (IFR6)

Note that the processor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low-order latch when the processor writes into the high-order counter.

In fact, it may not be necessary to write to the low-order counter in some applications since the timing operation is triggered by writing to the high-order counter.

The second set of addresses allows the processor to write into the latch register without affecting the count-down in progress. This is discussed in detail below.

READING THE TIMER 1 REGISTERS

For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows:

RS3	RS2	RS1	RS0	Operation (R/$\overline{W}$ = H)
L	H	L	L	Read T1 low-order counter. Reset T1 interrupt flag (IFR6)
L	H	L	H	Read T1 high-order counter.
L	H	H	L	Read T1 low-order latch.
L	H	H	H	Read T1 high-order latch.

TIMER 1 OPERATING MODES

Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are as follows:

ACR7 Output Enable	ACR6 "Free-Run" Enable	Mode
0	0	Generate a single time-out interrupt each time T1 is loaded. PB7 is disabled.
0	1	Generate continuous interrupts. PB7 is disabled.
1	0	Generate a single interrupt and an output pulse on PB7 for each T1 load operation.
1	1	Generate continuous interrupts and a square-wave output on PB7.

TIMER 1 ONE-SHOT MODE

The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval time, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7=1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

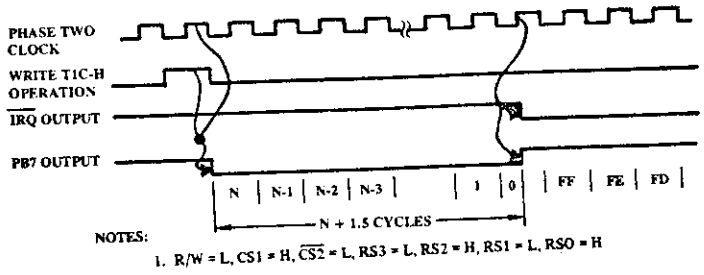
> NOTE
>
> The PB7 output enable function will over-ride bit 7 of the Data Direction Register B. PB7 will act as an output if DDRB7=1 <u>or</u> if ACR7=1.

In the one-shot mode, writing into the high-order latch has no effect on the operation of Timer 1. However, it will be necessary to assure that the low-order latch contains the proper data before initiating the countdown with a "write T1C-H" operation. When the processor writes into the high-order counter, T1L-H will also copy the data, the T1 interrupt flag will be cleared, the contents of the low-order latch will be transferred into the low-order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the phase two following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless a "write T1C-H" operation has taken place.

Timing for the R6522 interval timer one-shot mode is shown in Figure 6-7.

TIMER 1 FREE-RUNNING MODE

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and



Interval Timer "One-Shot" Mode Timing Sequence
FIGURE 6-7

the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

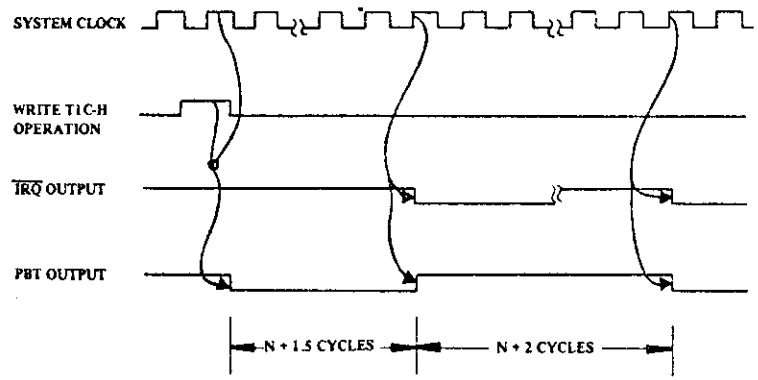
In the free-running mode (ACR6 = 1), the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described below. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the R6500 family devices are "re-triggerable." Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high-order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for

the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex pulse width modulated waveforms can be generated. Timing for the free-running mode is shown in Figure 6-8.

6.4.6 Timer 2

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high-order counter. The counter registers act as a 16-bit counter which decrements at $\phi 2$ rate.



Timer 1 Free-Running Mode
FIGURE 6-8

Timer 2 addressing can be summarized as follows:

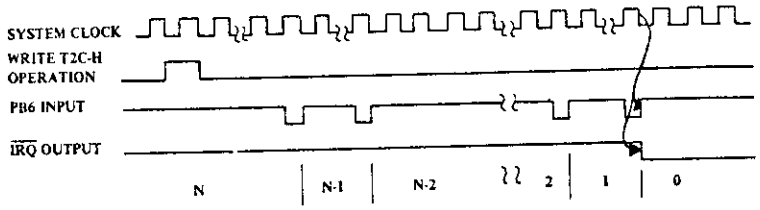
RS3	RS2	RS1	RS0	R/W = 0	R/W = 1
H	L	L	L	Write T2L-L	Read T2C-L Clear Interrupt flag
H	L	L	H	Write T2C-H Transfer T2L-L to T2C-L Clear Interrupt flag	Read T2C-H

TIMER 2 INTERVAL TIMER MODE

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 6-9.

TIMER 2 PULSE COUNTING MODE

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary



Timer 2 Pulse Counting Mode

FIGURE 6-9

to rewrite T2C-H to allow the interrupt flag to set on subsequent down-counting operations. Timing for this mode is shown in Figure 6-10.

6.4.7 Shift Register

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling shifting in external devices.

The control bits which allow control of the various shift register operating modes are located in the Auxiliary Control Register. These bits can be set and cleared by the system processor to select one of the operating modes discussed in the following paragraphs.

SHIFT REGISTER INPUT MODES

Auxiliary Control Register ACR4 selects the shift register input or output mode. There are three input modes and four output modes, differing primarily in the source of the pulses which control the shifting operation. With ACR4=0 the input modes are selected by ACR3 and ACR2 as follows:

ACR4	ACR3	ACR2	
0	0	0	Shift Register Disabled
0	0	1	Shift in under Control of Timer 2
0	1	0	Shift in at system clock rate
0	1	1	Shift in under Control of External Input Pulses

All Shift Register inputs are sampled into the Shift Register during the Ø2 low immediately following the detection of the shift clock rising transition. This detection occurs during Ø2 high.

MODE 000 - SHIFT REGISTER DISABLED

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operating is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

MODE 001 - SHIFT IN UNDER CONTROL OF TIMER 2

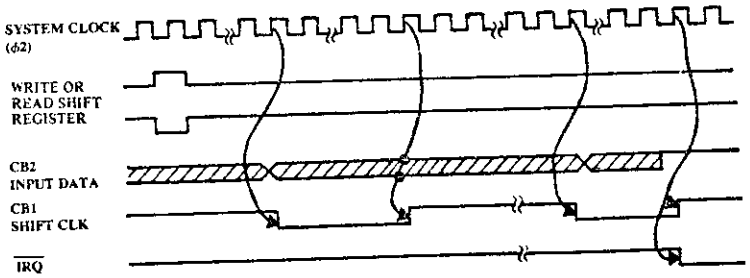
In this mode the shifting rate is controlled by the low-order eight

bits of T2. Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low-order T2 latch.

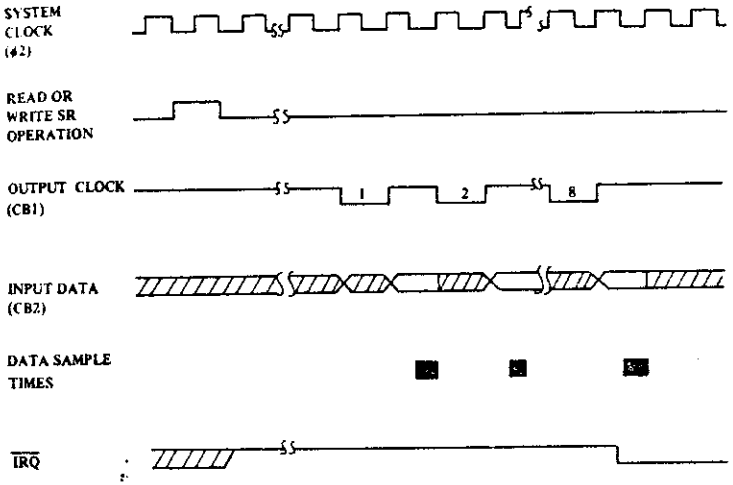
The shifting operation is triggered by writing or reading the Shift Register. Data are shifted first into the low-order bit of SR and are then shifted into the next-higher-order bit of the Shift Register on the trailing edge of each clock pulse. As shown in Figure 6-10, the input data should change on the negative edge of the clock pulse. These data are loaded into the Shift Register during the system clock cycle following the positive edge of the clock pulse. After eight clock pulses, the Shift Register Interrupt Flag will be set.

MODE 010 - SHIFT IN AT SYSTEM CLOCK RATE

In this mode the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. The shifting operation is triggered by reading or writing the Shift Register. Data are shifted first into bit 0 and are then shifted into the next-higher-order bit of the Shift Register on the positive edge of each clock pulse. After nine clock pulses, the Shift Register Interrupt Flag will be set, and the output clock pulses on CB1 will stop. Figure 6-11 illustrates this timing.



Shifting in Under Control of T2
FIGURE 6-10



Timing Sequence for Shifting in at System Clock Rate
FIGURE 6-11

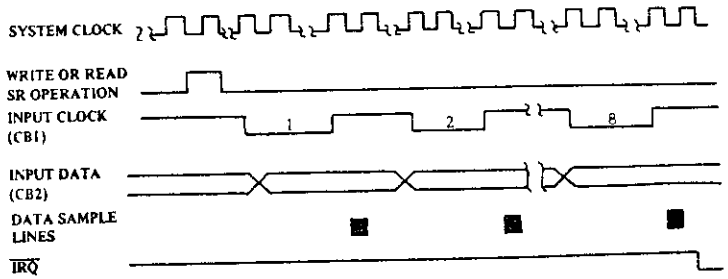
MODE 011 - SHIFT IN UNDER CONTROL OF EXTERNAL CLOCK

In this mode CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another eight pulses.

Note that data are shifted during the first system clock cycle following the positive edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. Timing for this operation is illustrated in Figure 6-12.

SHIFT REGISTER OUTPUT MODES

The four shift register output modes are selected by setting the input/output control bit (ACR4) to a logic 1 and then selecting the specific output mode with ACR3 and ACR2. In each of these modes the shift register shifts data out of bit 7 to the CB2 pin. At the same time the contents of bit 7 are shifted back into bit 0. As in the input modes, CB1 is used either



Timing Sequence for Shifting in Under Control of External Clock

FIGURE 6-12

as an output to provide shifting pulses out or as an input to allow shifting from an external pulse. The four modes are as follows:

ACR4	ACR3	ACR2	Mode
1	0	0	Shift Out - Free-Running Mode. Shift Rate Controlled by T2.
1	0	1	Shift Out - Shift Rate Controlled by T2.
1	1	0	Shift Out at System Clock Rate.
1	1	1	Shift Out Under Control of an External Pulse.

All shift register outputs are set during Ø2 low immediately following the transition (falling) of the shift clock 1. This occurs during Ø2 high.

MODE 100 FREE-RUNNING OUTPUT

This mode is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into

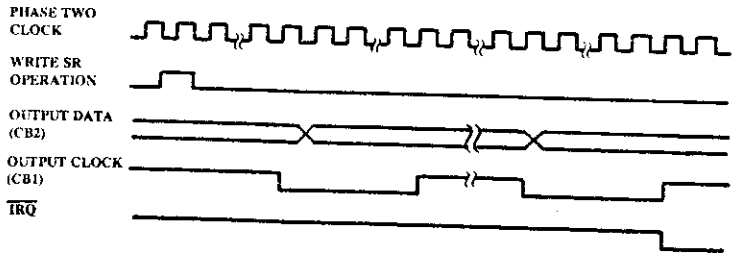
bit 0, the eight bits loaded into the Shift Register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

MODE 101 - SHIFT OUT UNDER CONTROL OF TIMER 2

In this mode the shift rate is controlled by Timer 2. However, with each read or write of the Shift Register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, eight shift pulses are generated on CB1 to control shifting in external devices. After the eight shift pulses, the shifting is disabled, and the SR Interrupt Flag is set. If the Shift Register is reloaded before the last time-out, the shifting will continue. This sequence is illustrated in Figure 6-13.

MODE 110 - SHIFTING OUT AT SYSTEM CLOCK RATE

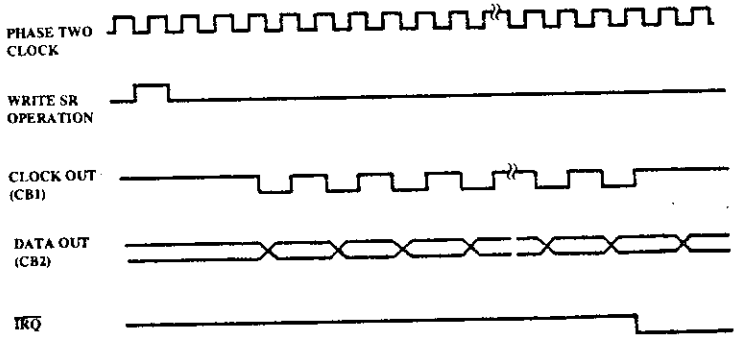
In this mode the shift register operation is similar to that of mode 101. However, the shifting rate is a function of the system clock on the chip enable pin (Ø2) and is independent of T2. Timer 2 resumes its normal function as an independent interval timer. Figure 6-14 illustrates the timing sequence for mode 110.



NOTE: DATA OUT DETERMINED BY CB2 CONTROL IN PCR:

Shifting Out Under Control of T2

FIGURE 6-13



Shifting Out Under Control of System Clock

FIGURE 6-14

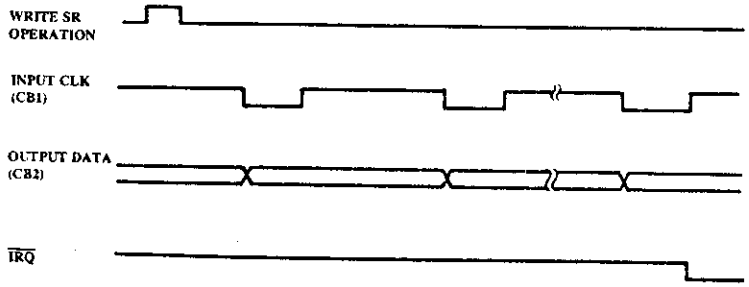
MODE 111 - SHIFT OUT UNDER CONTROL OF AN EXTERNAL PULSE

In this mode, shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts eight pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR Counter is initialized to begin couting the next eight shift pulses on pin CB1. After eight shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

Figure 6-15 illustrates the timing sequence for mode 111.

6.4.8 Interrupt Control

Controlling interrupts within the R6522 involves three principal operations: flagging the interrupts, enabling interrupts, and signalling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must



Shifting Out Under Control of External Clock

FIGURE 6-15

examine these flags in order from highest to lowest priority. This is accomplished by reading the flag reigster into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This bit can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-or'ed" with other devices in the system to interrupt the processor.

In the R6522, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This permits very convenient polling of several devices within a system to locate the source of an interrupt.

	7	6	5	4	3	2	1	0
Interrupt Flag Register	IRQ	T1	T2	CB1	CB2	SR	CA1	CA2
Interrupt Enable Register	Set/ clear control	T1	T2	CB1	CB2	SR	CA1	CA2

INTERRUPT FLAG REGISTER

The IFR is a read/limited write register. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: IRQ = IFR6 X IER6 + IFR5 X IER5 + IFR4 X IER4 + IFR3 X IER3 + IFR2 X IER2 + IFR1 X IER1 + IFR0 X IER0.

Note: X = logic AND, + = Logic OR.

Bits six through zero are latches which are set and cleared as follows:

Bit #	Set by	Cleared by
0	Active transition of the signal on the CA2 pin.	Reading or writing the A Port Output Register (ORA) using address 0001.
1	Active transition of the signal on the CA1 pin.	Reading or writing the A Port Output Register (ORA), using address 0001.
2	Completion of eight shifts	Reading or writing the Shift Register.
3	Active transition of the signal on the CB2 pin.	Reading or writing the B Port Output Register.
4	Active transiton of the signal on the CB1 pin.	Reading or writing the B Port Output Register.
5	Time-out of Timer 2.	Reading T2 low order counter or writing T2 high order counter.
6	Time-out of Timer 1.	Reading T1 low order counter or writing T1 high order latch

In addition to the clearing operations shown in the table, individual bits in the IFR can be cleared by writing into the register. A logic 1 in the data word written into the IFR will clear the corresponding interrupt flag. A zero in this word will leave the corresponding flag untouched. Setting the flags occurs only from interrupting conditions within the chip.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

INTERRUPT ENABLE REGISTER (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register (IER). The system processor can set or clear selected bits in this register to facilitate controling individual interrupts without affecting others. If bit 7 of the data placed on the system data bus during the write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register. Bit 7 will be read as a logic 0.

6.4.9 Function Control

Control of the various functions and operating modes within the R6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR), and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the interval timers (T1, T2), and the serial port (SR).

PERIPHERAL CONTROL REGISTER

The Peripheral Control Register is organized as follows:

Bit No.	7	6	5	4	3	2	1	0
Function	CB2 Control			CB1 Control	CA2 Control			CA1 Control

Each of these functions is discussed in detail below.

1. CA1 Control

Bit 0 of the Peripheral Control Register selects the active transition of the input signal applied to the CA1 interrupt input pin. If this bit is a logic 0, the CA1 interrupt flag will be set by a negative transition (high to low) of the signal on the CA1 pin. If PCR0 is a logic 1, the CA1 interrupt flag will be set by a positive transition (low to high) of this signal.

2. CA2 Control

The CA2 pin can be programmed to act as an interrupt input or as a peripheral control output. As an input, CA2 operates in two modes, differing primarily in the methods available for resetting the interrupt flag. Each of these two input modes can operate with either a positive or a negative active transition as described above for CA1.

In the output mode, the CA2 will perform either a "Read" or a "write" handshake operation. The CA2 operating modes are selected as follows:

PCR3	PCR2	PCR1	Mode
0	0	0	CA2 Negative Edge Interrupt (IFR0/ORA Clear) Mode -- Set CA2 interrupt flag (IFR0) on a negative transition of the input signal. Clear IFR0 on a read or write of the Peripheral A Output Register (ORA) or by writing logic 1 into IFR0.
0	0	1	CA2 Negative Edge Interrupt (IFR0 Clear) Mode -- Set IFR0 on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag. Clear IFR0 by writing logic 1 into IFR0.
0	1	0	CA2 Positive Edge Interrupt (IFR0/ORA Clear) Mode -- Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFR0 with a read or write of the Peripheral A Output Register.
0	1	1	CA2 Positive Edge Interrupt (IFR0 Clear) Mode -- Set IFR0 on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag. Clear IFR0 by writing logic 1 into IFR0.
1	0	0	CA2 Handshake Output Mode -- Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1.
1	0	1	CA2 Pulse Output Mode -- CA2 goes low for one cycle following a read or write of the Peripheral A Output Register.
1	1	0	CA2 Output Low Mode -- The CA2 output is held low in this mode.
1	1	1	CA2 Output High Mode -- The CA2 output is held high in this mode.

In the interrupt-IFR0 clear input mode, writing or reading the ORA register has no effect on the CA2 interrupt flag. This flag must be cleared by writing a logic 1 into the appropriate IFR bit. This mode allows the processor to handle interrupts which are independent of any operations taking place on the peripheral I/O ports.

The handshake and pulse output modes have been described previously. Note that the timing of the output signal varies [illegible] depending on whether the operation is initiated by a read or write.

3. CB1 Control

Control of the active transition [illegible]

is a logic 1, the CB1 interrupt flag (IFR4) is a logic 1, the CB1 interrupt flag (IFR4) will be set by a negative transition of the CB1 input signal and cleared by a read or write of the ORB register. If PCR4 is a logic one, IFR4 will be set by a positive transition of CB1.

If the Shift Register function has been enabled, CB1 will act as an input or output for the shift register clock signals. In this mode, the CB1 interrupt flag will still respond to the selected transition of the signal on the CB1 pin.

4. CB2 Control

With the serial port disabled, operation of the CB2 pin is a function of the three high-order bits of the PCR. The CB2 modes are very similar to those described previously for CA2. These modes are selected as follows:

PCR7	PCR6	PCR5	Mode
0	0	0	CB2 Negative Edge Interrupt (IFR3/ORB Clear) Mode -- Set CB2 interrupt flag (IFR3) on a negative transition of the CB2 input signal. Clear IFR3 on a read or write of the Peripheral B Output Register (ORB) or by writing logic 1 into IFR3.
0	0	1	CB2 Negative Edge Interrupt (IFR3 Clear) Mode -- Set IFR3 on a negative transition of the CB2 input signal. Reading or writing ORB does not clear the interrupt flag. Clear IFR3 by writing logic 1 into IFR3.
0	1	0	CB2 Positive Edge Interrupt (IFR3/ORB Clear) Mode -- Set CB2 input signal. Clear the CB2 interrupt flag on a read or write of ORB or by writing logic 1 into IFR3.
0	1	1	CB2 Positive Edge Interrupt (IFR3 Clear) Mode -- Set IFR3 on a positive transition of the CB2 input signal. Reading or writing ORB does not clear the CB2 interrupt flag. Clear IFR3 by writing logic 1 into IFR3.
1	0	0	CB2 Handshake Output Mode -- Set CB2 low on a write ORB operation. Reset CB2 high with an active transition of the CB1 input signal.
1	0	1	CB2 Pulse Output Mode -- Set CB2 low for one cycle following a write ORB operation.
1	1	0	CB2 Manual Output Low Mode -- The CB2 output is held low on this mode.
1	1	1	CB2 Manual Output High Mode -- The CB2 output is held high in this mode.

AUXILIARY CONTROL REGISTER

Many of the functions in the auxiliary control register have been discussed previously. However, a summary of this register is presented here as a convenient reference for the R6522 user. The auxiliary control register is organized as follows:

Bit No.	7	6	5	4	3	2	1	0
Function	T1 Control		T2 Control	Shift Register Control			PB Latch Enable	PA Latch Enable

1. PA Latch Enable

The R6522 provides input latching on both the PA and PB ports. In this mode, the data present on the peripheral A input pins will be latched within the chip when the CA1 interrupt flag is set. Reading the PA port will result in these latches being transferrred into the processor. As long as the CA1 interrupt flag is set, the data on the peripheral pins can change without affecting the data in the latches. This input latching can be used with any of the CA2 input or output modes.

It is important to note that on the PA port, the processor always reads the data on the peripheral pins (as reflected in the latches). For output pins, the processor still reads the latches. This may or may not reflect the data currently in the ORA. Proper system operation requires careful planning on the part of the system designer if input latching is combined with output pins on the peripheral ports.

Input latching is enabled by setting bit 0 in the Auxiliary Control Register to a logic 1. As long as this bit is a 0, the latches will directly reflect the data on the pins.

2. PB Latch Enable

Input latching on the PB port is controlled in the same manner as that described for the PA port. However, with the peripheral B port the input latch will store either the voltage on the pin or the contents of the Output Register (ORB) depending on whether the pin

is programmed to act as an input or an output. As with the PA port, the processor always reads the input latches.

3. Shift Register Control

The Shift Register operating mode is selected as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift register disabled.
0	0	1	Shift in under control of Timer 2.
0	1	0	Shift in under control of Ø2 pulses.
0	1	1	Shift in under control of external clock pulses.
1	0	0	Free-running output at rate determined by Timer 2.
1	0	1	Shift out under control of Timer 2.
1	1	0	Shift out under control of the Ø2 pulses.
1	1	1	Shift out under control of external clock pulses.

4. T2 Control

Timer 2 operates in two modes. If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

5. T1 Control

Timer 1 operates in the one-shot or free-running mode with the PB7 output control enabled or disabled. These modes are selected as follows:

ACR7	ACR6	Mode
0	0	One-Shot Mode -- Output to PB7 disabled.
0	1	Free-Running Mode -- Output to PB7 disabled.
1	0	One-Shot Mode -- Output to PB7 enabled.
1	1	Free-Running Mode -- Output to PB7 enabled.

6.5 R6522 APPLICATION NOTES

The R6522 represents a significant advance in general-purpose microprocessor I/O. Unfortunately, its many powerful features coupled with a set of very flexible operating modes, cause this device to appear to be very complex at first glance. However, a detailed analysis will show that the VIA is organized to allow convenient control of these powerful features. This section seeks to assist the system designer in his understanding of the R6522 by illustrating how the device can be used in microprocessor-based systems.

6.5.1 Control of R6522 Interrupts

Organization of the R6522 interrupt flags into a single register greatly facilitates the servicing of interrupts from this device. Since there is only one IRQ output for the seven possible sources of interrupt within the chip, the processor must examine these flags to determine the cause of an interrupt. This is best accomplished by first transferring the contents of the flag register into the accumulator. At this time it may be necessary to mask off those flags which have been disabled in the Interrupt Enable Register. This is particularly important for the edge detecting inputs where the flags may be set whether or not the interrupting function has been enabled. Masking of those flags can be accomplished by performing an AND operation between the IER and the accumulator or by performing an "AND IMMEDIATE." The second byte of this AND # instruction should specify those flags which correspond to interrupt functions which are to be serviced.

If the N flag is set after these operations, an active interrupt exists within the chips. This interrupt can be detected with a series of shift and branch instructions.

Clearing interrupt flags is accomplished very conveniently by writing a logic 1 directly into the appropriate bit of the Interrupt Flag Register. This can be combined with an interrupt enable or disable operation as follows:

```
        LDA #%10010000 ; initialize accumulator
        STA IFR        ; clear interrupt flag
        STA IER        ; set interrupt enable flag

or      LDA #%00001000 ; initialize accumulator
        STA IFR        ; clear interrupt flag
        STA IER        ; disable interrupt
```

Another very useful technique for clearing interrupt flags is simply to transfer the contents of the flag register back into this register as follows:

```
LDA IFR ; transfer IFR to accumulator
STA IFR ; clear flags corresponding to active interrupts
```

After completion of this operation the accumulator will still contain the interrupt flag information. Most importantly, writing into the flag register clears only those flags which are already set. This eliminates the possibility of inadvertently clearing a flag while it is being set.

6.5.2 Use of Timer 1

Timer 1 represents one of the most powerful features of the R6522 The ability to generate very evenly spaced interrupts and the ability to control the voltage on PB7 makes this timer particularly valuable in various timing, data detection and waveform generation applications.

TIME-OF-DAY CLOCK APPLICATIONS

An important feature of many systems is the time-of-day clock. In microprocessor-based systems the time of day is usually maintained in memory and is updated in an interrupt service routine. A regular processor interrupt will then assure that this time of day will always be available when it is needed in the main program.

Generating very regular interrupts using previously available timers presented difficulties because of the need to reload the timer for each interrupt. Unfortunately, the time between the interrupts will fluctuate due to variations in the interrupt response time. This problem is eliminated in the Timer 1 "free-running" mode. The accuracy of these "free-running" interrupts is only a function of the system clock and is not affected by interrupt response time.

ASYNCHRONOUS DATA DETECTION

The extraction of clock and data information from serial asynchronous ASCII signals or from any single channel data recording device relies on the ability to establish accurate strobes. As discussed previously, the period of these strobes can be seriously affected by the interrupt response time using conventional timers. However, T1 again allows generation of very accurate interrupts. The processor responds to these interrupts by strobing

the input data. The ability to reload the T1 latches without affecting the count-down in progress is very useful in this application. This allows the strobe time to be doubled or halved during data detection.

Figure 6-16 is an example of the use of this timer with asynchronous serial data.

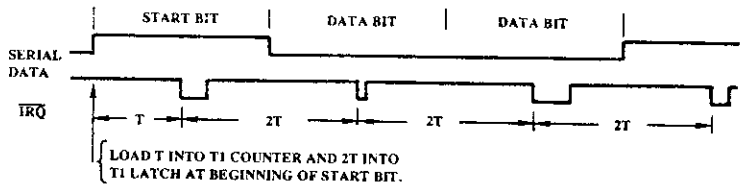
WAVEFORM GENERATION WITH TIMER 1

In addition to generating processor interrupts, Timer 1 can be used to control the output voltage on peripheral pin PB7 (output mode). In this mode a single negative pulse can be generated on PB7 (one-shot mode) or, in the free-running mode, a continuous waveform can be generated. In this latter mode the voltage on PB7 will be inverted each time T1 times out.

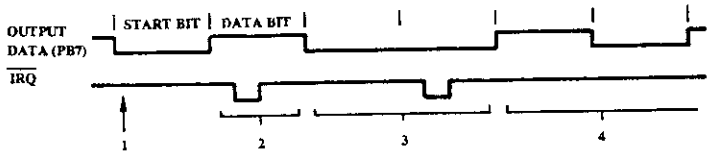
A single solenoid can be triggered by simply writing to T1C-H in the one-shot mode if the PB7 signal is used to control the solenoid directly.

Generating very complex waveforms can be a simple problem if T1 is used to control PB7 in the free-running mode. During any count-down process the latches can be loaded to determine the length of the next count-down period.

Figure 6-17 shows this timing sequence for generating ASCII serial data.



Asynchronous Data Detection Using Timer 1
FIGURE 6-16



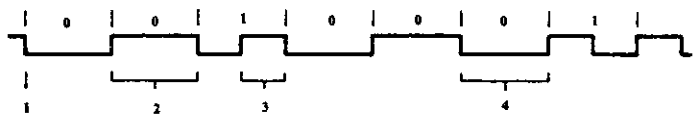
1. LOAD T INTO T1 COUNTER AND LATCH. LOAD T INTO T2 TO TRIGGER T1 LATCH RELOAD.
2. LOAD 2T INTO T1 LATCH DURING THIS BIT TIME.
3. LOAD T INTO T1 LATCH ANYTIME DURING THIS PERIOD. LOAD NT INTO T2. N = NUMBER OF 1'S AND 0'S WHICH FOLLOW.
4. A SERIES OF 1'S AND 0'S WILL BE GENERATED UNTIL THE T1 LATCH IS AGAIN CHANGED. NOTE THAT THE USE OF T2 TO CONTROL RELOADING THE T1 LATCH ELIMINATES THE NEED TO INTERRUPT ON EACH TRANSITION.

ASCII Serial Data Generation Using T1

FIGURE 6-17

An application where this mode of operation is also very powerful is in the generation of biphase encoded data for tape or disk storage. This encoding technique and the sequence of operations which would take place illustrated in Figure 6-18.

These applications represent only a tiny portion of the potential T1 applications. Some other possibilities are pulse width modulation waveforms, sound generation for video games, and A/D techniques requiring very accurate pulse widths.



1. LOAD T1 COUNTER AND LATCH.
2. SHIFT T1 LATCH ONE BIT TO THE RIGHT DURING THIS PERIOD.
3. SHIFT T1 LATCH LEFT DURING THIS PERIOD.
4. SHIFT T1 LATCH RIGHT DURING THIS PERIOD.

NOTE THAT T1 MUST BE ACCESSED ONLY WHEN THE OUTPUT DATA CHANGES. A STRING OF 1'S OR 0'S CAN BE GENERATED WITHOUT PROCESSOR INTERVENTION.

Generating Biphase Encoded Data

FIGURE 6-18

SECTION 7

R6530 ROM — RAM — I/O TIMER (RRIOT)

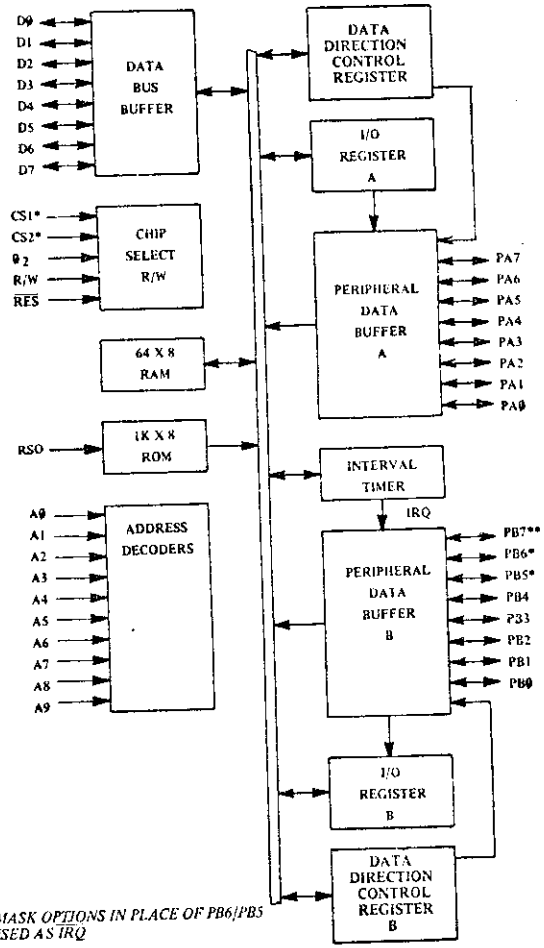
The R6530 is designed to operate in conjunction with the R650X Microprocessor (CPU). It is comprised of a mask-programmable 1024 x 8 ROM; a 64 x 8 RAM; two 8-bit bidirectional ports, capable of directly interfacing the Microprocessor unit and peripheral devices; and a programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

The I/O configuration, the interval timer and interrupt capability are under software control.

- 8-bit bidirectional Data Bus for communication with the microprocessor unit
- Two 8-bit bidirectional ports for direct interface to peripherals
- Two Programmable Data Direction Registers
- Programmable Interval Timer from 1 to 256 x 1024 clock periods.
- Programmable interval Timer Interrupt
- TTL and CMOS-Compatible Peripheral Lines
- Peripheral Pins with Direct Transistor Drive Capability
- Three-State Data Pins
- Up to 7K contiguous ROM with no external decoding
- 1024 x 8 ROM
- 64 x 8 Static RAM

7.1 R6530 ORGANIZATION

A block diagram of the internal architecture is shown in Figure 7-1 The R6530 is divided into four basic sections, RAM, ROM, I/O and TIMER. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit [illegible]. Each half contains a Data Direction Register (DDR) and an I/O Register. The DDR controls the peripheral output buffers. A "1" written into the [illegible] the corresponding peripheral buffer as an output buffer [illegible]



R6530 Internal Architecture

FIGURE 7-1

anything then written into the I/O Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the I/O Register. The output buffer remains in the high state, making it ready to receive data on the peripheral lines.

It should be noted that the microprocessor, when reading the I/O Register, is in fact reading the Peripheral Pin and not the I/O Register. The only way the I/O Register data can be changed is by a microprocessor Write operation. The Register is not affected by the data on the Peripheral Pin.

7.1.1 ROM -- 1K Byte (8K Bits)

The 8K ROM is in a 1024 x 8 configuration. Address lines A0-A9, as well as RSØ are needed to address the entire ROM. With the addition of CS1 and CS2, up to seven R6530s may be addressed, giving 7168 x 8 bits of contiguous ROM.

7.1.2 RAM -- 64 Bytes (512 Bits)

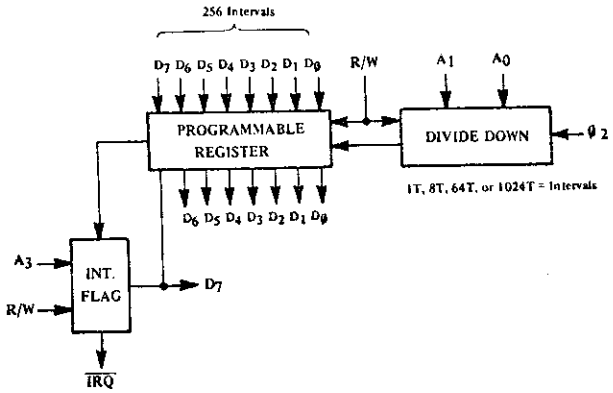
A 64 x 8 static RAM is contained on the R6530. It is addressed by A0-A5 (Byte Select), RS0, A6, A7, A8, A9 and, depending on the number of chips in the system, CS1 and CS2.

7.1.3 Internal Peripheral Registers

There are four internal registers, two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of data into and out of the peripheral pins. For example, a "1" loaded into data direction register A, position 3 sets up peripheral pin PA3 as an output. If a "0" had been loaded instead, PA3 would be configured as an input. The two output registers are used to latch data from the data bus during a Write operation until the peripheral device can read the data supplied by the microprocessor unit. Although during a Read operation the microprocessor unit reads the peripheral pin, the address is the same as the register. For those pins programmed as outputs by the data direction registers, the data on the pins will be the same as in the I/O register.

7.1.4 Interval Timer

The Timer section of the R6530 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 7-2.



Basic Elements of Interval Timer

FIGURE 7-2

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1." After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

When writing to the timer, the high-order 8 bits of the timer are written by the system data bus. If a count of 52 time intervals were to be counted, 0 0 1 1 0 1 0 0 would be written into the timer section. The time intervals of 1, 8, 64 or 1024T are decoded from address lines AØ and A1 at this same time. Address line A3, if high during this write operation, enables the interrupt flag onto pin PB7. PB7 should be programmed as an input if it is to be used as a interrupt pin. PB7 goes low when an interrupt occurs. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

Should the timer be read when interrupt occurs, the value read would be 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If, after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read = 1 1 1 0 0 1 0 0

Complement = 0 0 0 1 1 0 1 1

ADD 1 = 0 0 0 1 1 1 0 0 = 28.

Thus, to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (= 52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After interrupt, whenever the timer is written or read the interrupt is reset. However, the reading or writing of the timer at the same time interrupt occurs will not reset the interrupt flag.

Figure 7-3 illustrates an example of interrupt.

When reading the timer after an interrupt, A3 should be low to disable the $\overline{IRQ}$ pin. This is done to avoid future interrupts until after another Write timer operation.

7.2 INTERFACE LINES

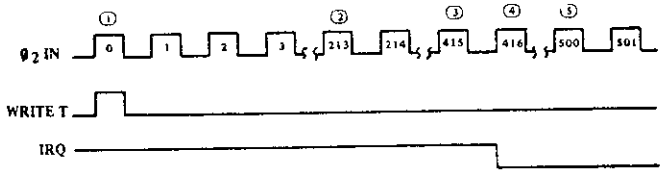
Figure 7-4 is the pinout diagram of the R6530.

7.2.1 Reset (RES)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all I/O registers. This in turn will cause all I/O buses to act as inputs, thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt is disabled when reset. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

7.2.2 Input Clock

The input clock is a system Phase Two clock which can be either a low-level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or a high-level clock ($V_{IL} < 0.2$, $V_{IH} = Vcc \begin{smallmatrix}+0.3\\-0.2\end{smallmatrix}$).



SHOULD THE PROGRAMMABLE TIMER REGISTER BE READ AT THE TIMES NOTED ON THE DIAGRAM ABOVE, IT WOULD CONTAIN:

① Data written into interval timer is 00110010 = 52_{10} A divide by 8 pre-scale is used.
② 00011001 = 25_{10} $52 - \frac{213}{8} - 1 = 52 - 26 - 1 = 25$
③ 00000000 = 0_{10} $52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$
④ Interrupt has occurred at Ø2 pulse #416
⑤ 10101100 Two: complement = 01010100 = 84_{10} $84 + (52 \times 8) = 500_{10}$

Example of Interrupt Generated by Interval Timer

FIGURE 7-3

7.2.3 Read/Write (R/W)

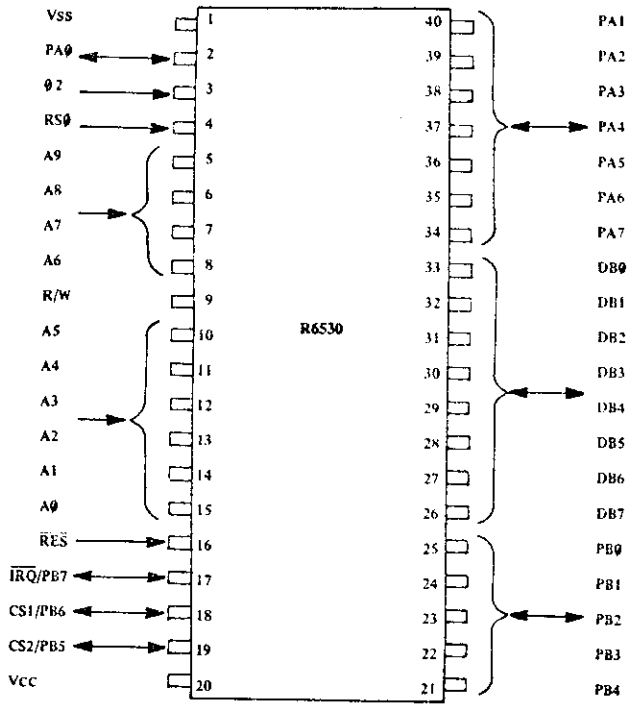
The R/W signal is supplied by the microprocessing unit and is used to control the transfer of data to and from the microprocessing unit and the R6530. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6530. A low on the R/W pin allows a write (with proper addressing) to the R6530.

7.2.4 Interrupt Request (IRQ)

The $\overline{IRQ}$ pin is an interrput pin from the interval timer. This same pin, if not used as an interrupt, can serve as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the data direction register. The pin will be normally high with a low indicating an interrupt from the R6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pull-up may be omitted with a mask option.

7.2.5 Data Bus (D0-D7)

The R6530 has eight bidirectional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from



R6530 Pinout Designation

FIGURE 7-4

the microprocessor unit. The output buffers remain in the "off" state except when a Read operation occurs.

7.2.6 Peripheral Data Ports

The R6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0-PA7 and PB0-PB7. PB5, PB6 and PB7 also have other uses which will be discussed in Section 7.3. The pins are set up as an input by writing a "0" into the corresponding bit in the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the R6530 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PA0 and PB0 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.

7.2.7 Address Lines (A0-A9)

There are 10 address pins. In addition to these 10, there is the ROM SELECT pin. The above pins, A0-A9 and ROM SELECT, are always used as addressing pins. There are two additonal pins which are mask-programmable and can be employed either individually or together as CHIP SELECTs. They are pins PB5 and PB6. When used as peripheral data pins they cannot be used as chip selects.

7.3 ADDRESSING

Addressing of the R6530 offers many variations to the user for greater flexibility. The user may configure his system with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0-A9). In addition, there is the possibility of three additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are chip-selects 1 and 2 (CS1 and CS2). The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering

the part. Both pins act independently of each other in that either or both pins may be designated as a chip-select. The third additional address line is RS0. The R6502 and R6530 in a 2-chip system would use RS0 to distinguish between ROM and non-ROM sections of the R6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Below is an example of a 1-chip and a 7-chip R6530 Addressing Scheme.

7.3.1 One-Chip Addressing

Figure 7-5 illustrates a 1-chip system decode for the R6530.

7.3.2 Seven-Chip Addressing

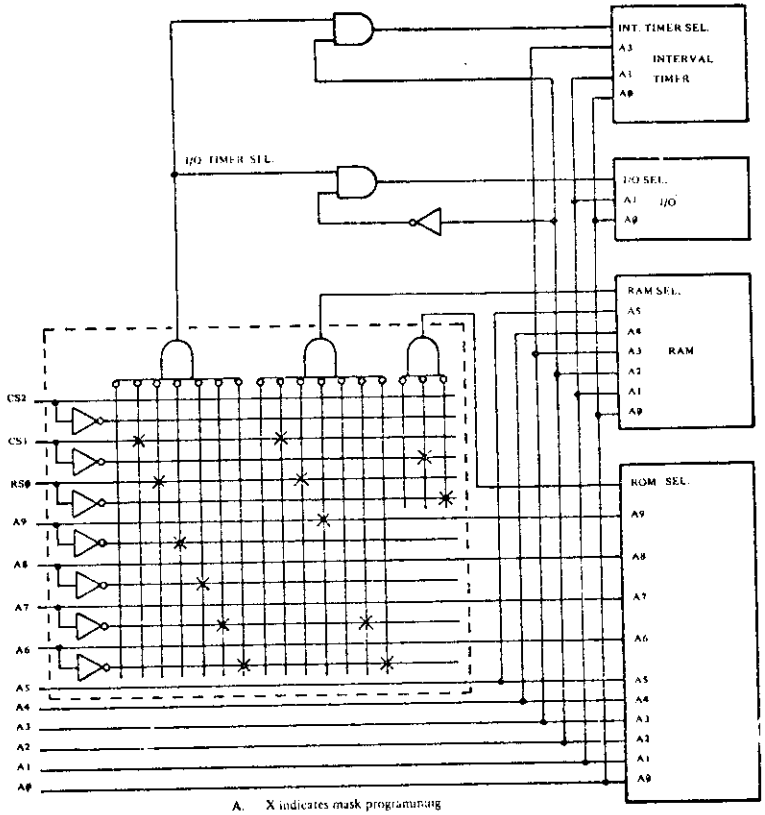
In the 7-chip system the objective would be to have 7K of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,536 and 1024. For this case, assume A13, A14 and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between Addresses 65,535 and 57,367. The 2 pins designated as chip-select or I/O would be masked programmed as chip-select pins. Pin RS0 would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12, respectively. (See Table 7-I).

The two examples given would permit addressing of the ROM and RAM; however, once the I/O timer has been addressed, further decoding is necessary to select which of the I/O registers are desired, as well as the coding of the interval timer.

7.3.3 I/O Register -- Timer Addressing

Table 7-2 illustrates the addressing decoding for the internal elements and timer programming. Address line A2 distinguishes I/O registers from the timer. When A2 is low and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected, A1 and A0 decode the divide by matrix. This is discussed further in the Timer Selection. In addition, Address A3 is used to enable the interrupt flag to PB7.



A. X indicates mask programming
i.e. ROM select = CS1•RSO
RAM select = $\overline{CS1}$•$\overline{RSO}$•A9•A7•A6
I/O TIMER SELECT = $\overline{CS1}$•$\overline{RSO}$•A9•A8•A7•A6

B. Notice that A8 is a "don't care" for RAM select

C. CS2 can be used as PB5 in this example.

R6530 One Chip Address Encoding Diagram
FIGURE 7-5

The addressing of the ROM select, RAM select and I/O Timer select lines would be as follows:

TABLE 7-1
Addressing Decode for I/O Register and Timer

		CS2 A12	CS1 A11	RSØ A10	A9	A8	A7	A6
R6530 #1,	ROM SELECT	0	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	0
	I/O TIMER	0	0	0	1	0	0	0
R6530 #2,	ROM SELECT	0	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	1
	I/O TIMER	0	0	0	1	0	0	1
R6530 #3,	ROM SELECT	0	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	0
	I/O TIMER	0	0	0	1	0	1	0
R6530 #4,	ROM SELECT	1	0	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	1
	I/O TIMER	0	0	0	1	0	1	1
R6530 #5,	ROM SELECT	1	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	0
	I/O TIMER	0	0	0	1	1	0	0
R6530 #6,	ROM SELECT	1	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	1
	I/O TIMER	0	0	0	1	1	0	1
R6530 #7,	ROM SELECT	1	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	1	0
	I/O TIMER	0	0	0	1	1	1	0

* RAM select for R6530 #5 would read = $\overline{A12}$•$\overline{A11}$•$\overline{A10}$•$\overline{A9}$•A8•$\overline{A7}$•$\overline{A6}$

TABLE 7-2
R6530 Seven-Chip Addressing Scheme

	ROM SELECT	RAM SELECT	I/O TIMER SELECT	R/W	A3	A2	A1	A0
	1	0	0	1	X	X	X	X
READ ROM	0	1	0	0	X	X	X	X
WRITE RAM	0	1	0	1	X	X	X	X
READ RAM	0	0	1	0	X	0	0	1
WRITE DDRA	0	0	1	1	X	0	0	1
READ DDRA	0	0	1	0	X	0	1	1
WRITE DDRB	0	0	1	1	X	0	1	1
READ DDRB	0	0	1	0	X	0	0	0
WRITE PER. REG. A	0	0	1	1	X	0	0	0
READ PER. REG. A	0	0	1	0	X	0	1	0
WRITE PER. REG. B	0	0	1	1	X	0	1	0
READ PER. REG. B	0	0	1	0	0	1	1	1
WRITE TIMER								
÷ 1T W/IRQ to PB7	0	0	1	0	1	1	0	0
÷ 8T WO/IRQ to PB7	0	0	1	0	0	1	0	1
÷ 64T W/IRQ to PB7	0	0	1	0	1	1	1	0
÷ 1024T WO/IRQ to PB7	0	0	1	0	0	1	1	1
READ TIMER DISABLE IRQ TO PB7	0	0	1	1	0	1	X	0
READ INTERRUPT FLAG	0	0	1	1	X	1	X	1

SECTION 8

R6532 RAM — I/O TIMER (RIOT)

The R6532 is designed to operate in conjunction with the R6500 Microcomputer System's microprocessor (CPU) family. It is comprised of a 128 x 8 static RAM; two software-controlled, 8-bit bidirectional data ports allowing direct interfacing between the microprocessor unit and peripheral devices; a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods; and a programmable edge-detecting circuit.

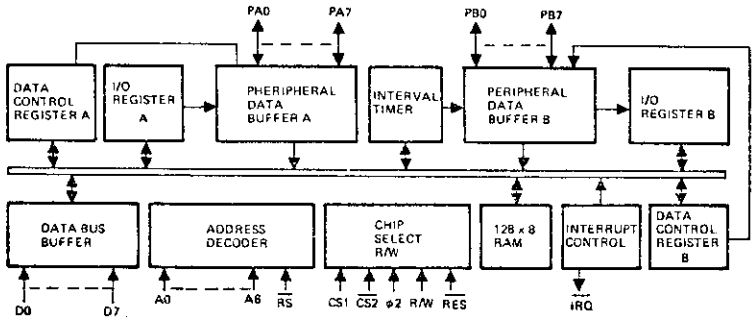
- 8-bit bidirectional Data Bus for direct communication with the microprocessor
- 128 x 8 static RAM
- Two 8 bit bidirectional data ports for interface to peripherals
- Two programmable Data Direction Registers
- Programmable Interval Timer with Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins
- Programmable edge-sensitive Interrupt

8.1 R6532 ORGANIZATION

A block diagram of the internal architecture is presented in Figure 8-1. The R6532 is divided into four basic sections, RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves, each of which contains a Data Direction Register (DDR) and an I/O Register.

8.1.1 RAM - 128 Bytes (1024 Bits)

The 128 x 8 Read/Write memory acts as a conventional [illegible] RAM. Data can be written into the RAM from the microprocessor [illegible] chip (CS1 = 1, $\overline{CS2}$ = Ø) and by setting $\overline{RS}$ to a logic [illegible] A[illegible] through A6 are then used to select the desired [illegible]



R6532 Internal Architecture

FIGURE 8-1

8.1.2 Internal Peripheral Registers

The Peripheral A I/O port consists of eight lines which can be individually programmed to act as either an input or an output. A logic 0 in a bit of the Data Direction Register (DDRA) causes the corresponding line of the PA port to act as an input. A logic 1 causes the corresponding PA line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Output Register (ORA).

Data are read directly from the PA pins during any read operation. For any output pin, the data transferred into the processor will be the same as those contained in the Output Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Output Register. This will not affect the polarity of the pin until the corresponding bit of DDRA is set to a logic 1 to allow the peripheral pin to act as an output.

The operation of the Peripheral B Input/Output port is exactly the same as the normal I/O operation of the Peripheral A port. The eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Output Register (ORB).

The primary difference between the PA and the PB ports is in the operation of the output buffers which drive these pins. The buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V. This allows these pins to directly drive transistor switches. To ensure that the microprocessor will read proper data on a "Read PB" operation, sufficient logic is provided in the chip to allow the microprocessor to read the Output Register instead of reading the peripheral pin as on the PA port.

8.1.3 Edge-Detecting Interrupt

In addition to acting as a peripheral I/O line, the PA7 line can serve as an edge-detecting input. In this mode, an active transition will set the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag will cause IRQ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge-detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable to disable interrupting of the processor. The data placed on the Data Bus during this operation are discarded and have no effect on the control of PA7.

Setting of the PA7 interrupt flag will occur on an active transition even if the pin is being used as a normal input or as a peripheral control output. The flag will also be set by an active transition if interrupting from PA7 is disabled. The reset signal ($\overline{RES}$) will disable the PA7 interrupt and will set the active transition to negative (high to low). During the system initialization routine, it is possible to set the interrupt flag by a negative transition. It may also be set by changing the polarity of the active interrupt. It is therefore recommended that the interrupt flag be cleared before enabling interrupting from PA7.

Clearing of the PA7 Interrupt Flag occurs when the microprocessor reads the Interrupt Flag Register.

8.1.4 Interval Timer

The Timer section (Figure 8-2) of the R6532 contains a preliminary divide-down register, a programmable 8-bit register, and interrupt logic.

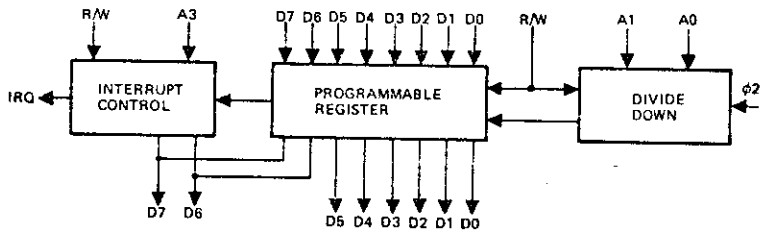
The Interval Timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic 1. After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the Timer will tell how long since the flag was set up to a maximum of 255T.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

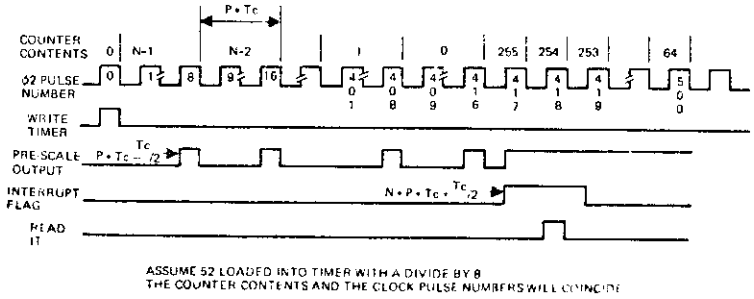
At the same time that data are being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e. $A_3 = 1$ enables $\overline{IRQ}$, $A_3 = 0$ disables $\overline{IRQ}$. When the the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the timer has counted thru 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is two's complement, but it should be remembered that interrupt occurred on count number -1 and we must, therefore, subtract 1:

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
ADD 1 = 0 0 0 1 1 1 0 0 = 28 Equals two's complement of register
SUB 1 = 0 0 0 1 1 0 1 1 = 27



Basic Elements of Interval Timer
FIGURE 8-2



Interval Timer Example
FIGURE 8-3

Thus, to arrive at the total elapsed time, one merely carries out a two's complement add to the original time written into the timer. Again, time is to be assumed to be written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 417T + 27T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (DB7 for the timer, DB6 for edge detect) data bus lines D0-D5 go to zero.

When reading the timer after an interrupt, A3 should be low to disable the $\overline{IRQ}$ pin. This is done to avoid future interrupts until after another Write timer operation.

8.2 INTERFACE LINES

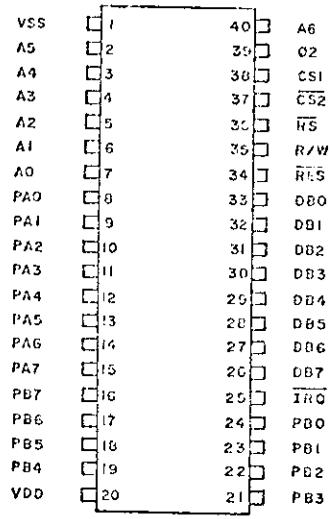
Figure 8-4 is the pinout diagram of the R6532

8.2.1 Reset (RES)

During system initialization a Logic "0" on the RES input will cause a zeroing of all four I/O registers. This, in turn, will cause all I/O buses to act as inputs, thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

8.2.2 Input Clock

The input clock is a system Phase 2 clock which can be either a low-level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or a high-level clock ($V_{IL} < 0.2$, $V_{IH} = Vcc\ ^{+0.3}_{-0.2}$).



R6532 Pinout Designation

FIGURE 8-4

8.2.3 Read/Write (R/W)

The R/W signal is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the R6532. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6532. A low on the R/W pin allows a write (with proper addressing) to the R6532.

8.2.4 Interrupt Request (IRQ)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high, with a low indicating an interrupt from the R6532. An external pull-up device is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

8.2.5 Data Bus (D0-D7)

The R6532 has eight bidirectional data pins (D0-D7). These pins connect to the system's data lines and permit transfer of data to and from the microprocessor array. The output buffers remain in the "off" state except when a Read operation occurs.

8.2.6 Peripheral Data Ports

The R6532 has 16 pins available for peripheral I/O operations. Each pin is individually software-programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0-PA7 and PB0-PB7. PB7 also has other uses which are discussed elsewhere. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the R6532 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PB0-PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.

8.2.7 Address Lines (A0-A6)

There are 7 address pins. In addition to these 7, there is the $\overline{\text{RAM SELECT}}$ pin. The above pins, A0-A6 and $\overline{\text{RAM SELECT}}$, are always used as addressing pins. There are two additional pins which are used as CHIP SELECTs. They are pins CS1 and $\overline{\text{CS2}}$.

8.3 ADDRESSING

Table 8-1 summarizes addressing decoding for the R6532.

TABLE 8-1

Addressing Decode for R6532

RAM ADDRESSING

$\overline{\text{RS}}$ = 0
RW = 1 to read, 0 to write
AØ-A6 select RAM address

I/O ADDRESSING

$\overline{\text{RS}}$ = 1 A2 = 0
RW = 1 to read, 0 to write

	A1	AØ
PA data	0	0
PA data direction	0	1
PB data	1	0
PB data direction	1	1

WRITE EDGE-DETECTION CONTROL

$\overline{\text{RS}}$, A2 = 1 R/W, A4 = 0

A1 = 1, enable interrupt from PA7
A1 = 0, disable interrupt from PA7
A0 = 1, positive edge detect
A0 = 0, negative edge detect

READ AND CLEAR INTERRUPT FLAG

$\overline{\text{RS}}$, R/W, A2, AØ = 1

Bit 7 = Timer Flag
Bit 6 = PA7 Flag

WRITE COUNT TO INTERVAL TIMER

$\overline{\text{RS}}$, A4, A2 = 1 R/W = 0

	A1	AØ
: 1	0	0
: 8	0	1
: 64	1	0
: 1024	1	1

A3 = 1 enable timer interrupt
A3 = 0 disable timer interrupt

NOTE: For all operations CS1 = 1, CS2 = 0.

APPENDIX A

SUMMARY OF SINGLE-CYCLE EXECUTION

This section contains an outline of the data on both the address bus and the data bus for each cycle of the various processor instructions. It tells the system designer exactly what to expect while single-cycling through a program.

Note that the processor will not stop in any cycle where R/W is a 0 (WRITE cycle). Instead, it will go right into the next READ cycle and stop there. For this reason, some instructions may appear to be shorter than indicated here.

All instructions begin with T0 and the fetch of the OP CODE and continue through the required number of cycles until the next T0 and the fetch of the next OP CODE.

While the basic terminology used in this appendix is discussed in the Programming Manual, it has been defined below for ease of reference while studying Single-Cycle Execution.

OP CODE--The first byte of the instruction containing the operator and mode of address.

OPERAND--The data on which the operation specified in the OP CODE is performed.

BASE ADDRESS--The address in Indexed addressing modes which specifies the location in memory to which indexing is referenced. The high-order byte of the base address (AB08 to AB15) is BAH (Base Address High) and the low-order byte of the base address (AB00 to AB07) is BAL (Base Address Low).

EFFECTIVE ADDRESS--The destination in memory in which data are to be found. The effective address may be loaded directly as in the case of Page Zero and Absolute Addressing or may be calculated as in Indexing operations. The high-order byte of the effective address (AB08 to AB15) is ADH and the low-order byte of the effective address (AB00 to AB07) is ADL.

INDIRECT ADDRESS--The address found in the operand of instructions utilizing (Indirect),Y which contains the low-order byte of the base address. IAH and IAL represent the high- and low-order bytes.

JUMP ADDRESS--The value to be loaded into Program Counter as a result of a Jump instruction.

A. 1. SINGLE-BYTE INSTRUCTIONS

ASL	DEX	NOP	TAX	TYA
CLC	DEY	ROL	TAY	
		ROR		
CLD	INX	SEC	TSX	
CLI	INY	SED	TXA	
CLV	LSR	SEI	TXS	

These single-byte instructions require two cycles to execute. During the second cycle the address of the next instruction in program sequence will be placed on the address bus. However, the OP CODE which appears on the data bus during the second cycle will be ignored. This same instruction will be fetched on the following cycle, at which time it will be decoded and executed. The ASL, ROL and LSR instructions apply to the accumulator mode of address.

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	OP CODE (Discarded)	1	
T0	PC + 1	OP CODE	1	Next Instruction

A. 2. INTERNAL EXECUTION ON MEMORY DATA

ADC	CMP	EOR	LDY
AND	CPX	LDA	ORA
BIT	CPY	LDX	SBC

The instructions listed above will execute by performing operations inside the microprocessor using data fetched from the effective address. This total operation requires three steps. The first step (one cycle) is the OP CODE fetch. The second (zero to four cycles) is the calculation of an effective address. The final step is the fetching of the data from the effective address. Execution of the instruction takes place during the fetching and decoding of the next instruction.

A. 2.1. Immediate Addressing (2 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	Data	1	Fetch Data
T0	PC + 2	OP CODE	1	Next Instruction

A. 2.2. Zero Page Addressing (3 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	ADL	1	Fetch Effective Address
T2	00, ADL	Data	1	Fetch Data
T0	PC + 2	OP CODE	1	Next Instruction

A. 2.3. Absolute Addressing (4 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	ADL	1	Fetch Low-Order Effective Address Byte
T2	PC + 2	ADH	1	Fetch High-Order Effective Address Byte
T3	ADH, ADL	Data	1	Fetch Data
T0	PC + 3	OP CODE	1	Next Instruction

A. 2.4. Indirect, X Addressing (6 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	BAL	1	Fetch Page Zero Base Address
T2	00, BAL	Data (Discarded)	1	
T3	00, BAL + X	ADL	1	Fetch Low-Order Byte of Effective Address
T4	00, BAL + X + 1	ADH	1	Fetch High-Order Byte of Effective Address
T5	ADH, ADL	Data	1	Fetch Data
T0	PC + 2	OP CODE	1	Next Instruction

A. 2.5. Absolute, X or Absolute, Y Addressing (4 or 5 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	BAL	1	Fetch Low-Order Byte of Base Address
T2	PC + 2	BAH	1	Fetch High-Order Byte of Base Address
T3	ADL: BAL + Index Register	Data*	1	Fetch Data (No Page Crossing)
	ADH: BAH + C			Carry is Ø or 1 as Required from Previous Add Operation
T4*	ADL: BAL + Index Register	Data	1	Fetch Data from Next Page
	ADH: BAH + 1			
T0	PC + 3	OP CODE	1	Next Instruction

*If the page boundary is crossed in the indexing operation, the data fetched in T3 is ignored. If page boundary is not crossed, the T4 cycle is bypassed.

A. 2.6. Zero Page, X or Zero Page, Y Addressing Modes (4 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	BAL	1	Fetch Page Zero Base Address
T2	00, BAL	Data (Discarded)	1	
T3	00, BAL + Index Register	Data	1	Fetch Data (No Page Crossing)
T0	PC + 2	OP CODE	1	Next Instruction

A. 2.7. Indirect, Y Addressing Mode (5 or 6 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	IAL	1	Fetch Page Zero Indirect Address
T2	00, IAL	BAL	1	Fetch Low-Order Byte of Base Address
T3	00, IAL + 1	BAH	1	Fetch High-Order Byte of Base Address
T4	ADL: BAL + Y ADH: BAH + C	Data*	1	Fetch Data from Same Page Carry is 0 to 1 as Required from Previous Add Operation
T5*	ADL: BAL + Y ADH: BAH + 1	Data	1	Fetch Data from Next Page
T0	PC + 2	OP CODE	1	Next Instruction

*If page boundary is crossed in indexing operation, the data fetch in T4 is ignored. If page boundary is not crossed, the T5 cycle is bypassed.

A. 3. STORE OPERATIONS

STA
STX
STY

The specific steps taken in the Store Operations are very similar to those taken in the previous group (internal execution on memory data). However, in the Store Operation, the fetch of data is replaced by a WRITE (R/W = 0) cycle. No overlapping occurs and no shortening of the instruction time occurs on indexing operations.

A. 3.1. Zero Page Addressing (3 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	ADL	1	Fetch Zero Page Effective Address
T2	00, ADL	Data	0	Write Internal Register to Memory
T0	PC + 2	OP CODE	1	Next Instruction

A. 3.2. Absolute Addressing (4 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	ADL	1	Fetch Low-Order Byte of Effective Address
T2	PC + 2	ADH	1	Fetch High-Order Byte of Effective Address
T3	ADH, ADL	Data	0	Write Internal Register to Memory
T0	PC + 3	OP CODE	1	Next Instruction

A. 3.3. Indirect, X Addressing (6 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	BAL	1	Fetch Page Zero Base Address
T2	00, BAL	Data (Discarded)	1	
T3	00, BAL + X	ADL	1	Fetch Low-Order Byte of Effective Address
T4	00, BAL + X + 1	ADH	1	Fetch High-Order Byte of Effective Address
T5	ADH, ADL	Data	0	Write Internal Register to Memory
T0	PC + 2	OP CODE	1	Next Instruction

A. 3.4. Absolute, X or Absolute, Y Addressing (5 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	BAL	1	Fetch Low-Order Byte of Base Address
T2	PC + 2	BAH	1	Fetch High-Order Byte of Base Address
T3	ADL: BAL + Index Register ADH: BAH + C	Data (Discarded)	1	
T4	ADH, ADL	Data	0	Write Internal Register to Memory
T0	PC + 3	OP CODE	1	Next Instruction

A. 3.5. Zero Page, X or Zero Page, Y Addressing Modes (4 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	BAL	1	Fetch Page Zero Base Address
T2	00, BAL	Data (Discarded)	1	
T3	ADL: BAL + Index Register	Data	0	Write Internal Register to Memory
T0	PC + 2	OP CODE	1	Next Instruction

A. 3.6. Indirect, Y Addressing Mode (6 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	IAL	1	Fetch Page Zero Indirect Address
T2	00, IAL	BAL	1	Fetch Low-Order Byte of Base Address
T3	00, IAL + 1	BAH	1	Fetch High-Order Byte of Base Address
T4	ADL: BAL + Y ADH: BAH	Data (Discarded)	1	
T5	ADH, ADL	Data	0	Write Internal Register to Memory
T0	PC + 2	OP CODE	1	Next Instruction

A. 4. READ -- MODIFY -- WRITE OPERATIONS

ASL LSR
DEC ROL
INC ROR

The Read -- Modify -- Write operations involve the loading of operands from the operand address, modification of the operand and the resulting modified data being stored in the original location.

A. 4.1. Zero Page Addressing (5 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	ADL	1	Fetch Page Zero Effective Address
T2	00, ADL	Data	1	Fetch Data
T3	00, ADL	Data	0	
T4	00, ADL	Modified Data	0	Write Modified Data Back into Memory
T0	PC + 2	OP CODE	1	Next Instruction

A. 4.2. Absolute Addressing (6 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	ADL	1	Fetch Low-Order Byte of Effective Address
T2	PC + 2	ADH	1	Fetch High-Order Byte of Effective Address
T3	ADH, ADL	Data	1	
T4	ADH, ADL	Data	0	
T5	ADH, ADL	Modified Data	0	Write Modified Data Back into Memory
TØ	PC + 3	OP CODE	1	Next Instruction

A. 4.3. Zero Page, X Addressing (6 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	BAL	1	Fetch Page Zero Base Address
T2	00, BAL	Data (Discarded	1	
T3	ADL: BAL + X (Without Carry)	Data	1	Fetch Data
T4	ADL: BAL + X (Without Carry)	Data	0	
T5	ADL: BAL + X (Without Carry)	Modified Data	0	Write Modified Data Back into Memory
TØ	PC + 2	OP CODE	1	Next Instruction

A. 4.4. Absolute, X Addressing (7 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	BAL	1	Fetch Low-Order Byte of Base Address
T2	PC + 2	BAH	1	Fetch High-Order Byte of Base Address
T3	ADL: BAL + X ADH: BAH + C	Data (Discarded)	1	
T4	ADL: BAL + X ADH: BAH + C	Data	1	Fetch Data
T5	ADH, ADL	Data	0	
T6	ADH, ADL	Modified Data	0	Write Modified Data Back into Memory
T0	PC + 3	OP CODE	1	New Instruction

A. 5. MISCELLANEOUS OPERATIONS

BCC	BRK	PHP
BCS	BVC	PLA
BEQ	BVS	PLP
BMI	JMP	RTI
BNE	JSR	RTS
BPL	PHA	

A. 5.1. Push Operation -- PHP, PHA (3 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	OP CODE (Discarded)	1	
T2	Stack Pointer*	Data	0	Write Internal Register into Stack
T0	PC + 1	OP CODE	1	Next Instruction

*Hereafter referrad to as "Stack Ptr."

A. 5.2. Pull Operations -- PLP, PLA (4 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	OP CODE (Discarded)	1	
T2	Stack Ptr.	Data (Discarded)	1	
T3	Stack Ptr. + 1	Data	1	Fetch Data from Stack
T0	PC + 1	OP CODE	1	Next Instruction

A. 5.3. Jump to Subroutine -- JSR (6 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	ADL	1	Fetch Low-Order Byte of Subroutine Address
T2	Stack Ptr.	Data (Discarded)	1	
T3	Stack Ptr.	PCH	0	Push High-Order Byte of Program Counter to Stack
T4	Stack Ptr. - 1	PCL	0	Push Low-Order Byte of Program Counter to Stack
T5	PC + 2	ADH	1	Fetch High-Order Byte of Subroutine Address
T0	Subroutine Address (ADH, ADL)	OP CODE	1	

A. 5.4. Break Operation -- (Hardware Interrupt)-BRK (7 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch BRK OP CODE (or Force BRK)
T1	PC + 1 (PC on Hardware Interrupt)	Data (Discarded)	1	
T2	Stack Ptr.	PCH	0	Push High-Order Byte of Program Counter to Stack
T3	Stack Ptr. - 1	PCL	0	Push Low-Order Byte of Program Counter to Stack
T4	Stack Ptr. - 2	P	0	Push Status Register to Stack
T5	FFFE (NMI-FFFA) (RES-FFFC)	ADL	1	Fetch Low-Order Byte of Interrupt Vector
T6	FFFF (NMI-FFFB) (RES-FFFD)	ADH	1	Fetch High-Order Byte of Interrupt Vector
T0	Interrupt Vector (ADH, ADL)	OP CODE	1	Next Instruction

A. 5.5. Return from Interrupt -- RTI (6 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	Data (Discarded)	1	
T2	Stack Ptr.	Data (Discarded)	1	
T3	Stack Ptr. + 1	Data	1	Pull P from Stack
T4	Stack Ptr. + 2	Data	1	Pull PCL from Stack
T5	Stack Ptr. + 3	Data	1	Pull PCH from Stack
T0	PCH, PCL	OP CODE	1	Next Instruction

A. 5.6. Jump Operation -- JMP

A.5.6.1. Absolute Addressing Mode (3 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	ADL	1	Fetch Low-Order Byte of Jump Address
T2	PC + 2	ADH	1	Fetch High-Order Byte of Jump Address
T0	ADH, ADL	OP CODE	1	Next Instruction

A.5.6.2. Indirect Addressing Mode (5 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	IAL	1	Fetch Low-Order Byte of Indirect Address
T2	PC + 2	IAH	1	Fetch High-Order Byte of Indirect Address
T3	IAH, IAL	ADL	1	Fetch Low-Order Byte of Jump Address
T4	IAH, IAL + 1	ADH	1	Fetch High-Order Byte of Jump Address
T0	ADH, ADL	OP CODE	1	Next Instruction

A. 5.7. Return from Subroutine -- RTS (6 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	Data (Discarded)	1	
T2	Stack Ptr.	Data (Discarded)	1	
T3	Stack Ptr. + 1	PCL	1	Pull PCL from Stack
T4	Stack Ptr. + 2	PCH	1	Pull PCH from Stack
T5	PCH, PCL (from Stack)	Data (Discarded)	1	
T0	PCH, PCL + 1	OP CODE	1	Next Instruction

A. 5.8. Branch Operation -- BCC, BCS, BEQ, BMI, BNE, BPL, BVC, BVS (2, 3, or 4 Cycles)

Tn	Address Bus	Data Bus	R/W	Comments
T0	PC	OP CODE	1	Fetch OP CODE
T1	PC + 1	Offset	1	Fetch Branch Offset
T2*	PC + 2 + Offset (w/o) Carry)	OP CODE	1	Offset Added to Program Counter
T3**	PC + 2 + Offset (with Carry)	OP CODE	1	Carry Added

*Skip if branch not taken.

**Skip if branch not taken; skip if branch operation does not cross page boundary.

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